

Compal confidential

Schematics Document

Mobile Yonah uFCPGA with Intel
Calistoga_GM/PM+ICH7-M core logic

2006-07-24
REV:1.0

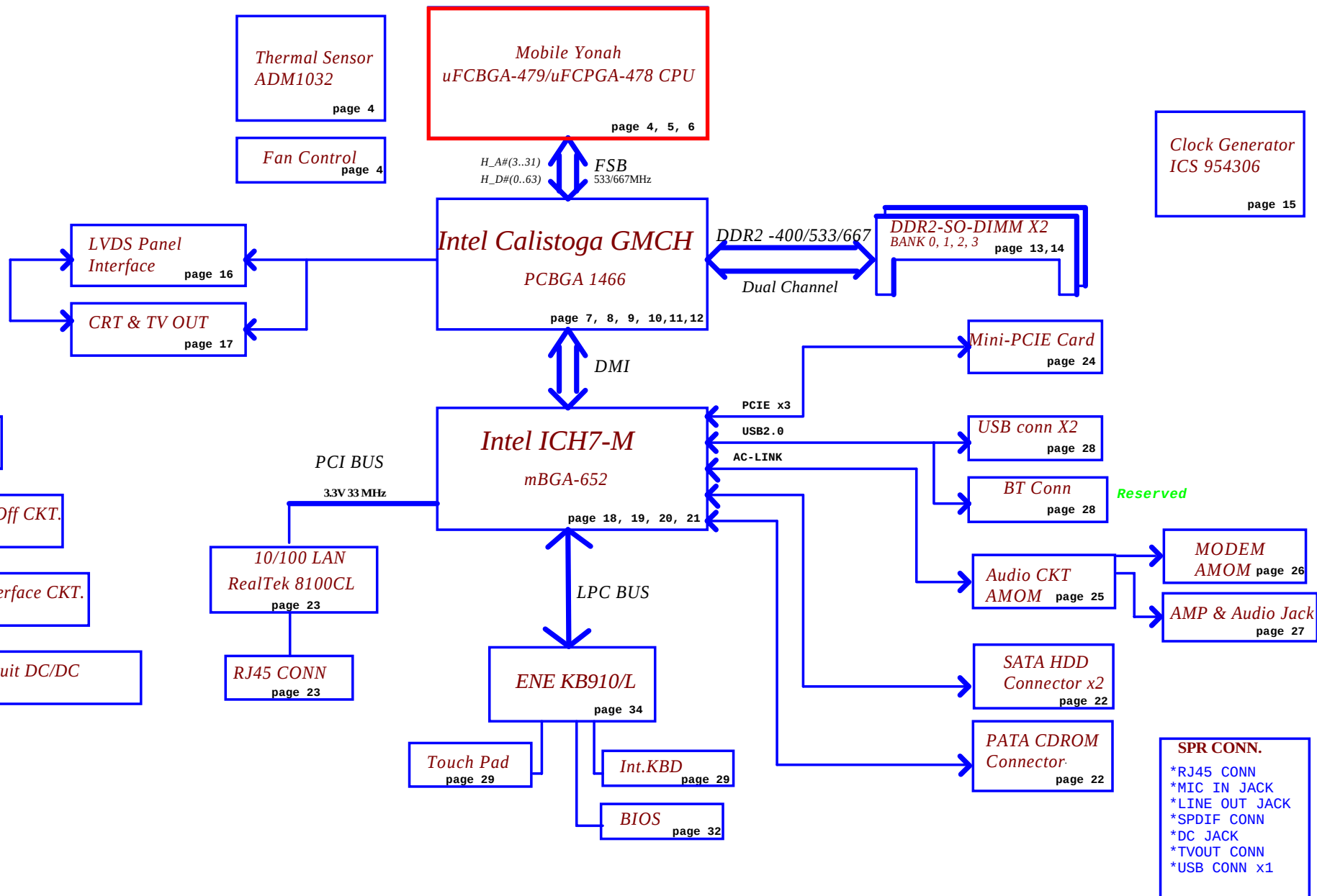
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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Cover Sheet	
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File Name : LA-3342P

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PCB



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				Block Diagram	

Voltage Rails

power plane State	+B LD03 LD05	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.5VS +0.9VS +CPU_CORE +VCCP
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

0 MEANS ON
X MEANS OFF

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G
RealTekK 8100CL	AD24	1	A

Load BOM check item

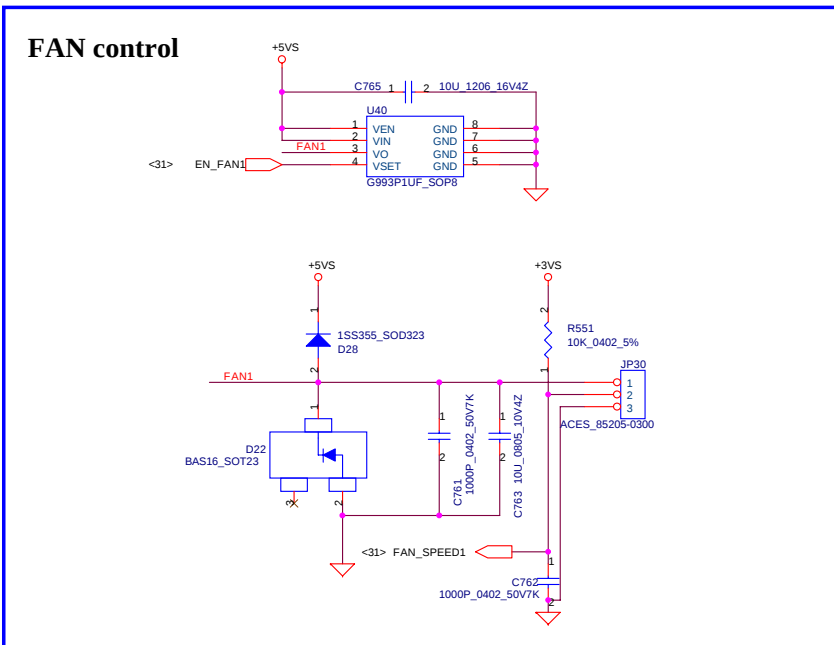
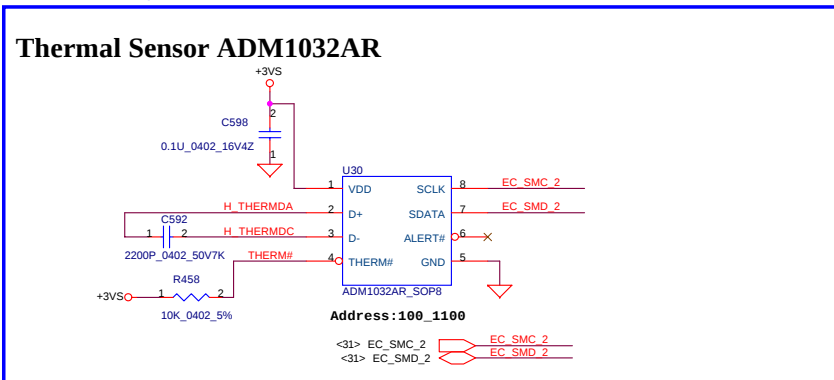
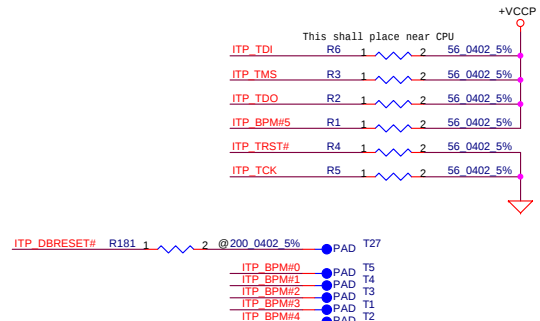
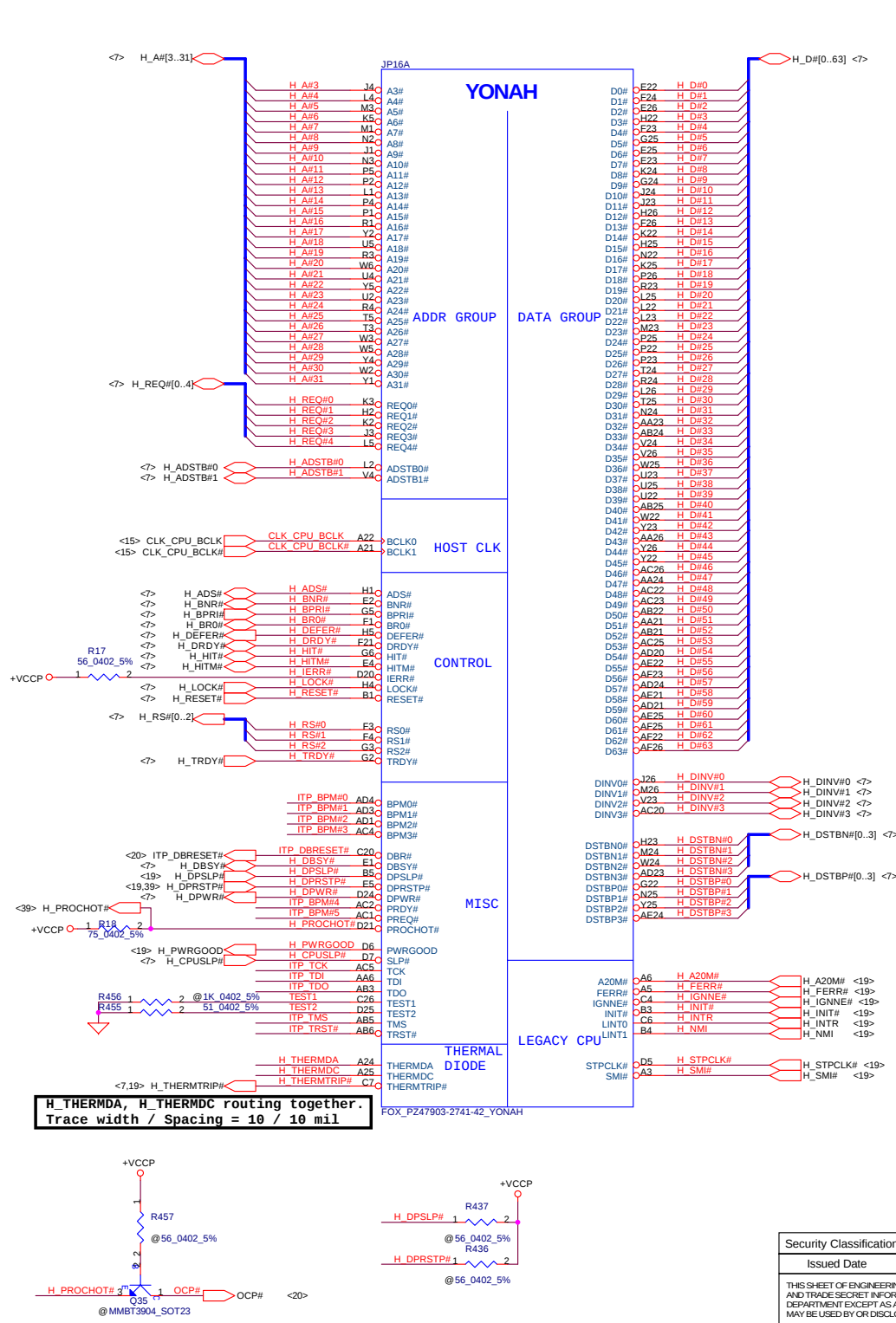
- 1.U31 GM/PM/GML part number
- 2.U6 ICH7 part number

BOM: 43144132L01 (GM)
43144132L02 (GML)

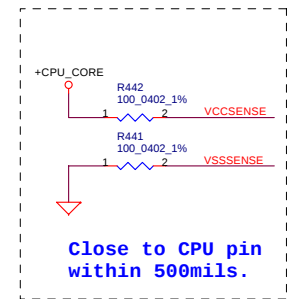
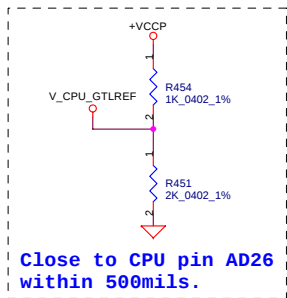
Jump-Short:

PJP4,PJP6,PJP7,PJP8,PJP10,PJP12,PJP14,PJP18,PJP19,PJP20,PJP25

MV step from PIRQE change to PIRQA for LAN poor performance.



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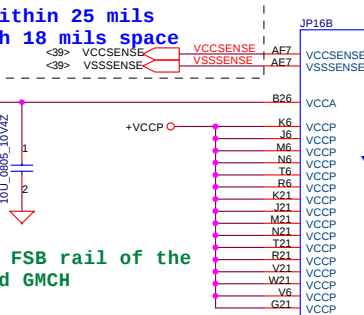
+1.5vs is a power source required by the PL clock generator on the processorsilicon

Length match within 25 mils
The trace width 18 mils space
7 mils

+VCCP is the FSB rail of the processor and GMCH

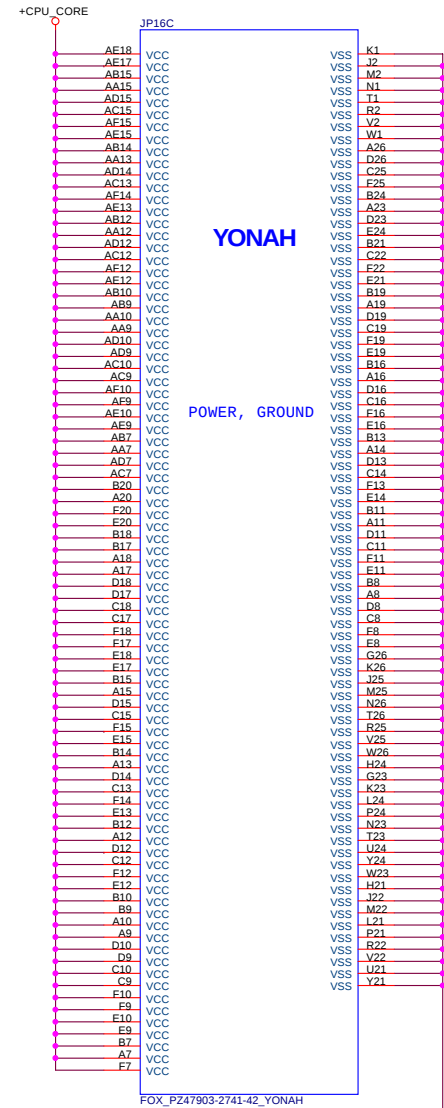
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal.



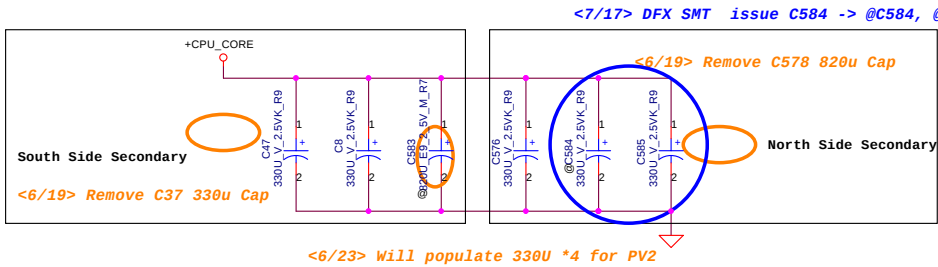
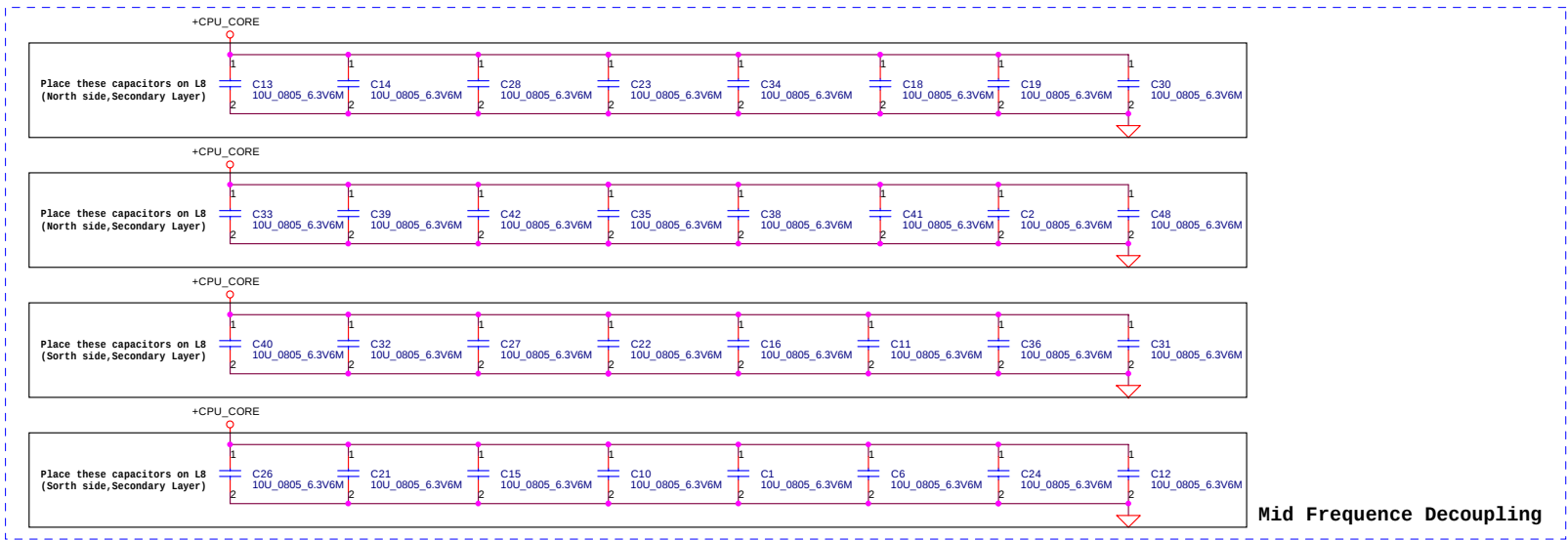
YONAH

POWER, GROUND, RESERVED SIGNALS AND NC

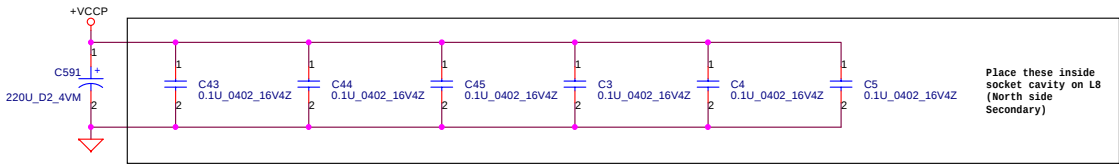


YONAH

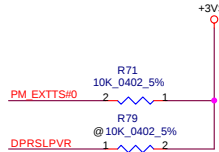
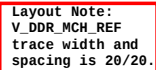
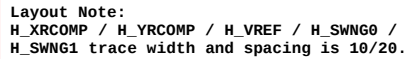
POWER, GROUND



ESR <= 1.5m ohm
Capacitor > 1980uF



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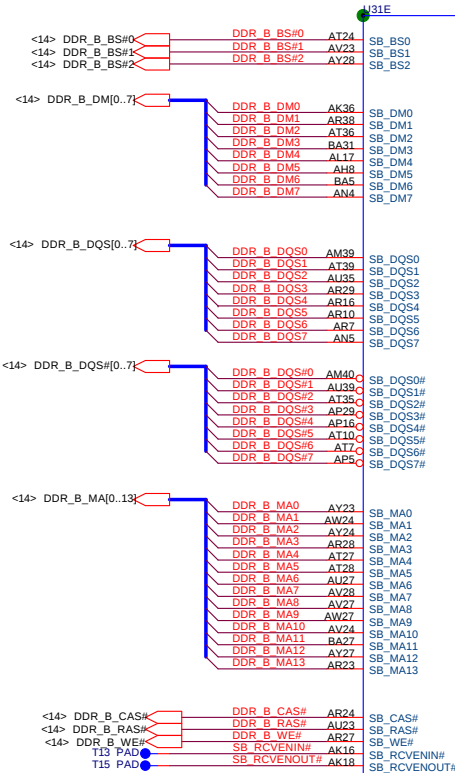
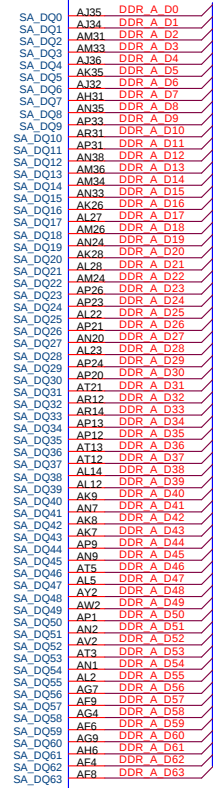


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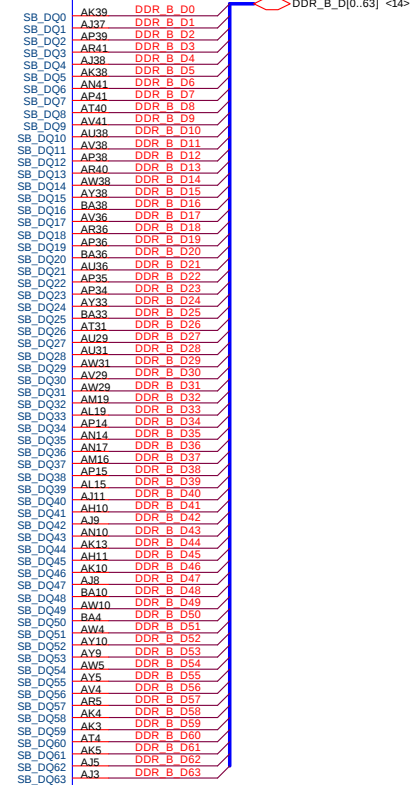
CALISTOGA_FCBGA1466-D

DDR SYS MEMORY A



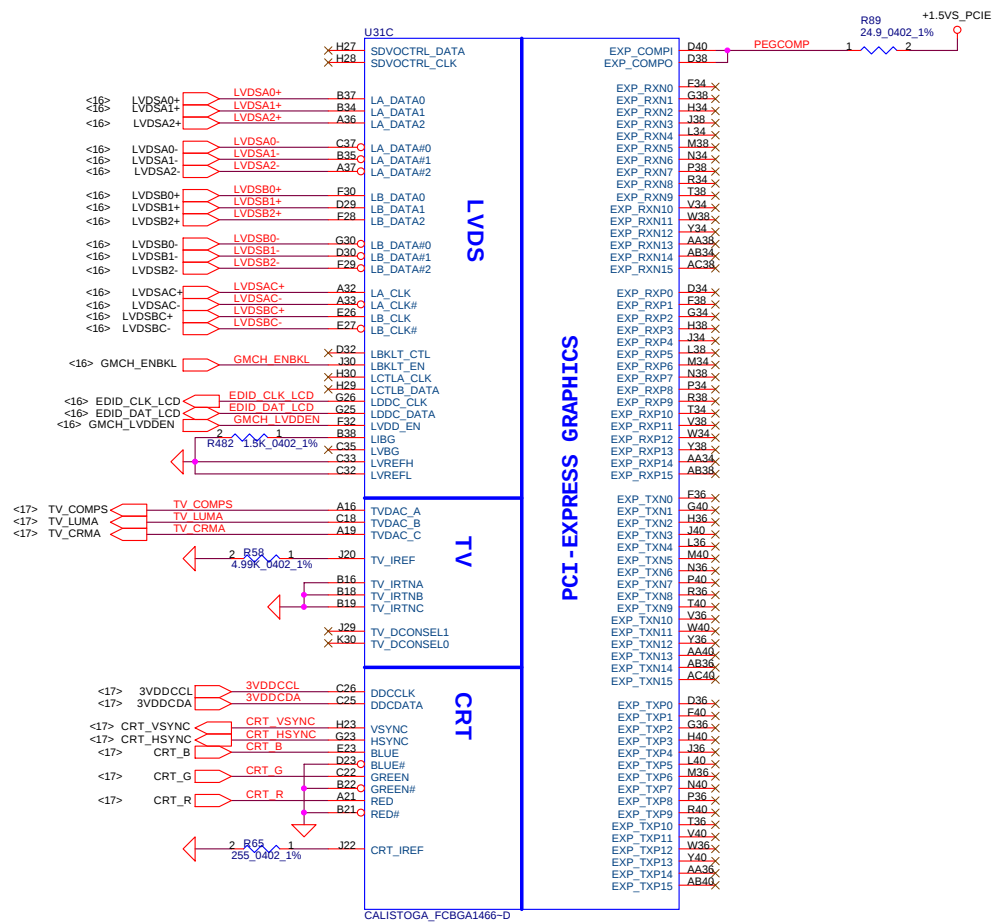
CALISTOGA_FCBGA1466-D

DDR SYS MEMORY B

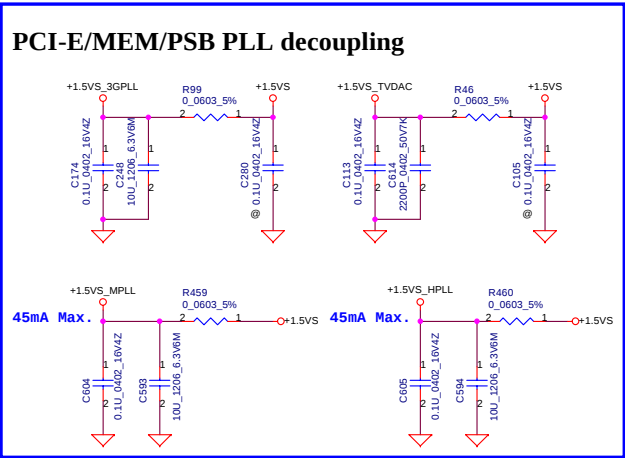
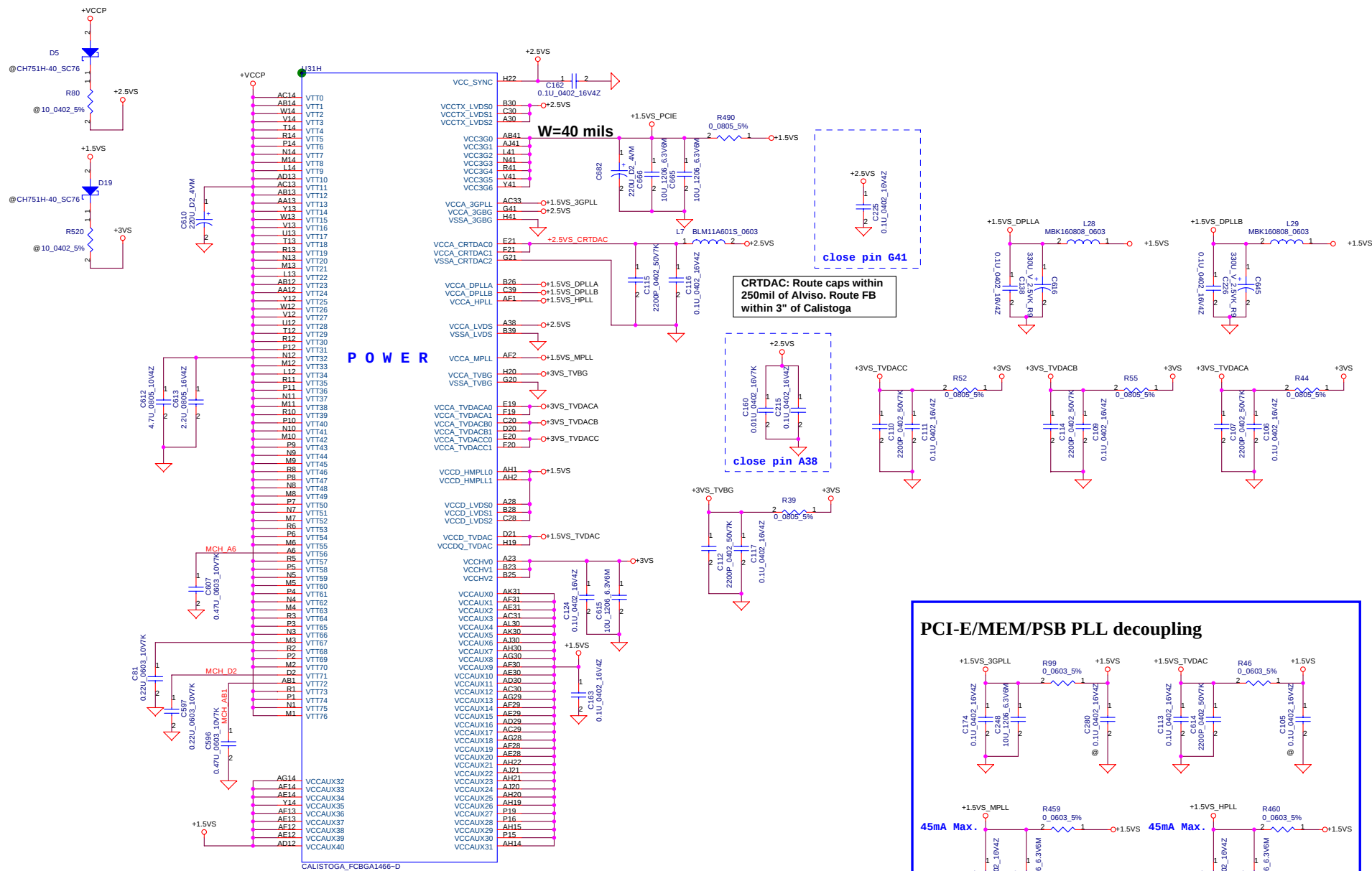


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Calistoga (2/6)



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Strap Pin Table

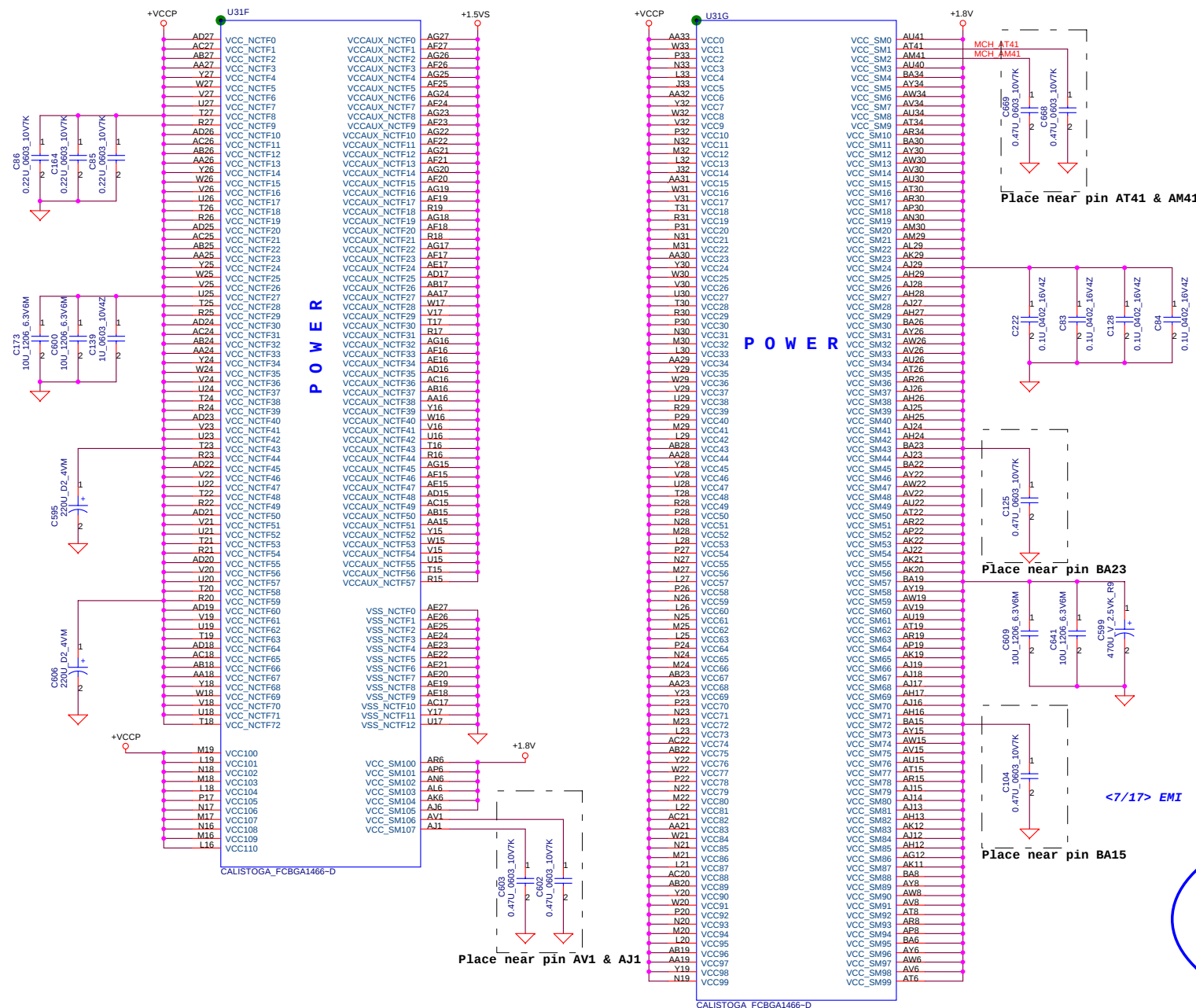
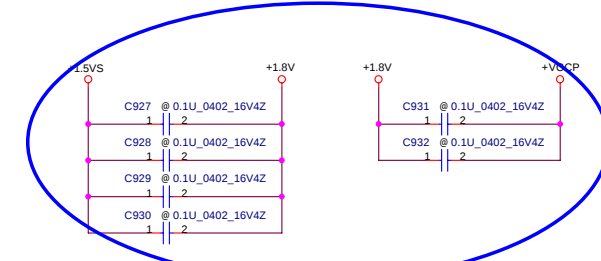
CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4*(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V*(Default) 01 = 1.5V
CFG19	0 = No SDVO Device Present *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

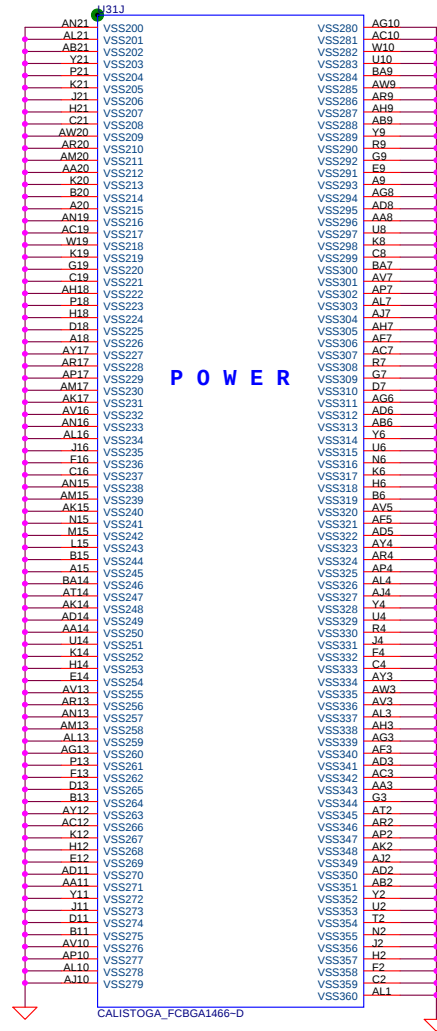
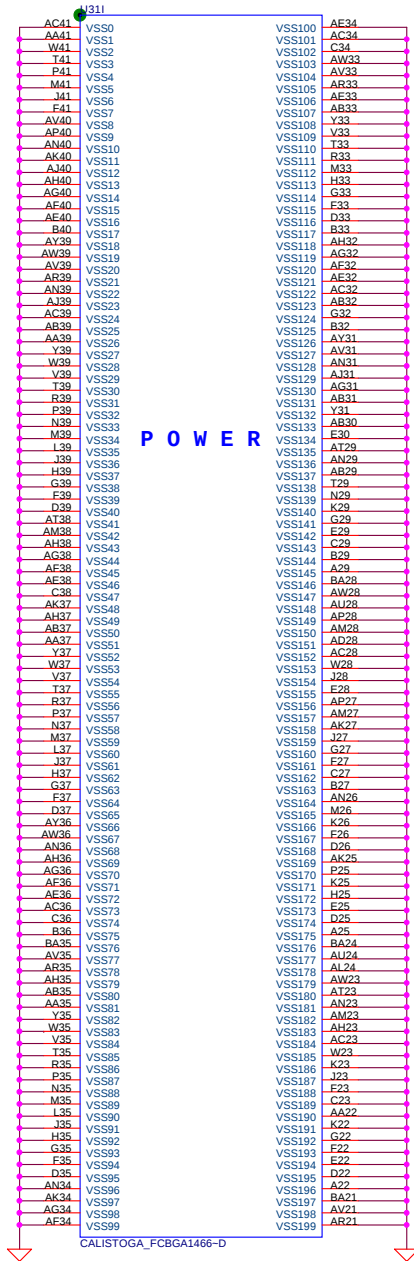
<7>	CFG5	R48	1	2	@ 2.2K 0402 5%
<7>	CFG7	R54	1	2	@ 2.2K 0402 5%
<7>	CFG9	R51	1	2	@ 2.2K 0402 5%
<7>	CFG11	R47	1	2	@ 2.2K 0402 5%
<7>	CFG12	R49	1	2	@ 2.2K 0402 5%
<7>	CFG13	R50	1	2	@ 2.2K 0402 5%
<7>	CFG16	R53	1	2	@ 2.2K 0402 5%

<7>	CFG18	R74	1	2	@ 1K 0402 5%
<7>	CFG19	R82	1	2	@ 1K 0402 5%
<7>	CFG20	R87	1	2	@ 1K 0402 5%

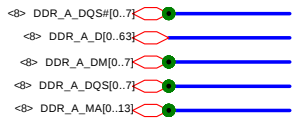
<7/17> EMI issue, add new parts C927,C928,C929,C930, C931,C932



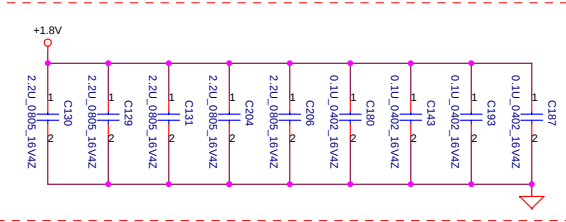
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				Calistoga (5/6)	



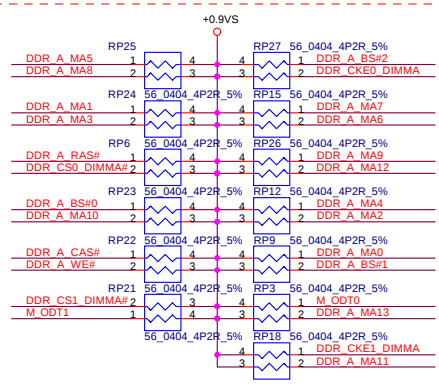
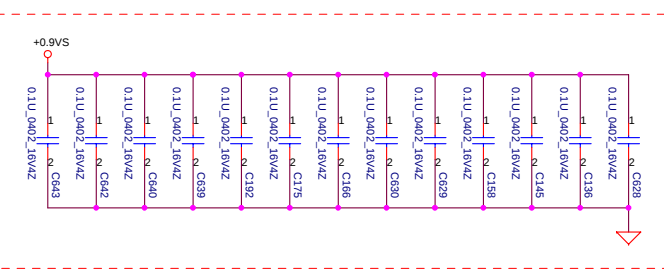
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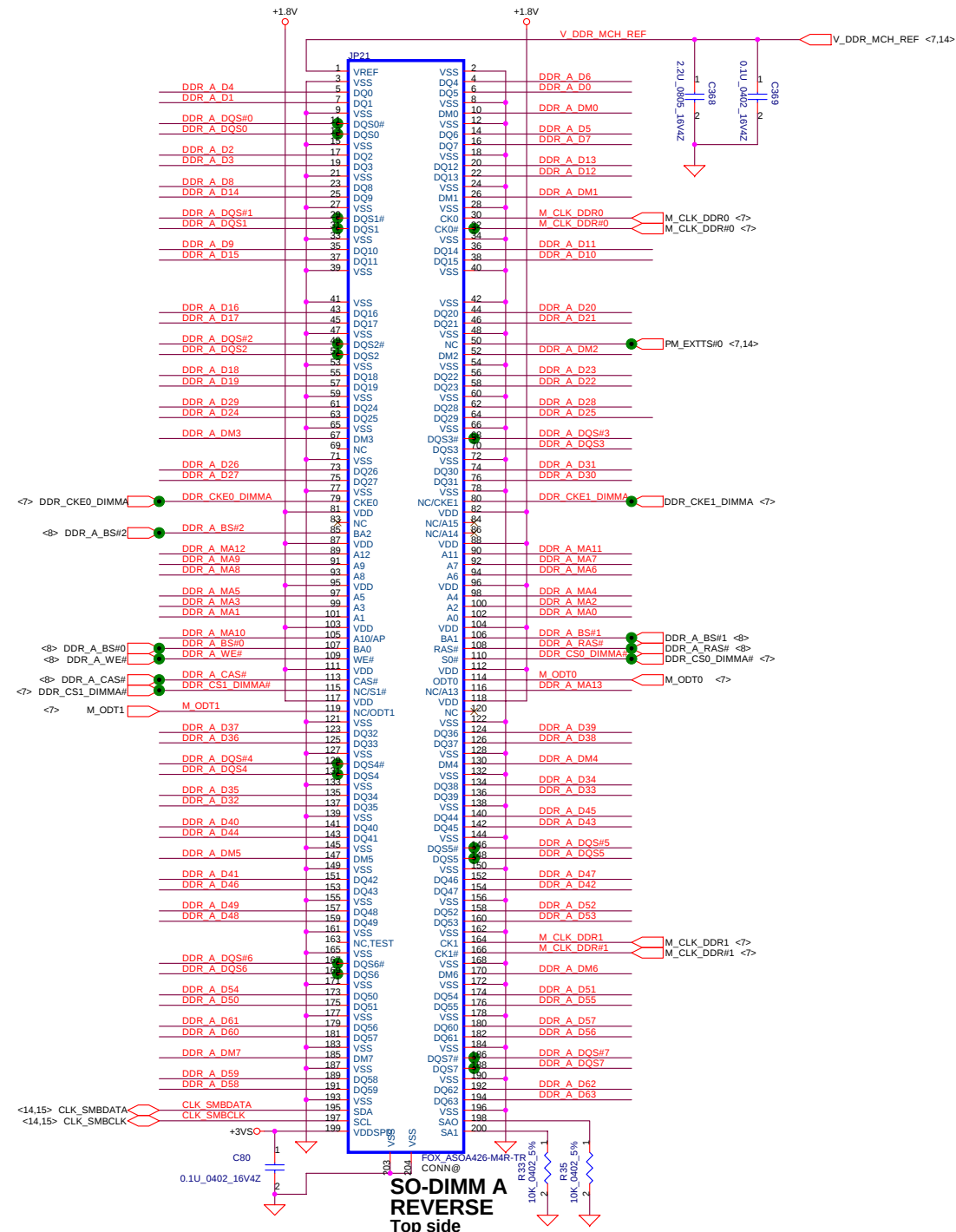
Layout Note:
Place near JP41



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP41,all trace length Max=1.5"



SO-DIMM A
REVERSE
Top side

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						DDRII-SODIMM SLOT1	
						Size	Rev
						Custom	0.1
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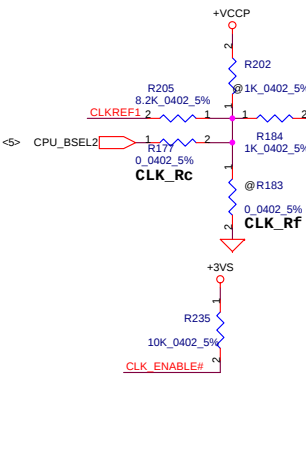
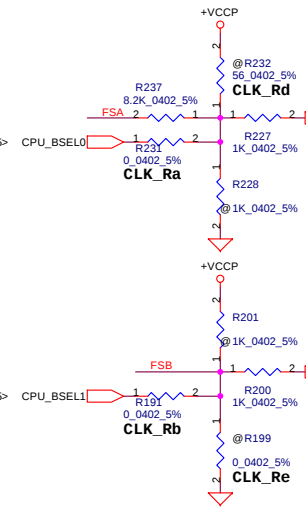
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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHZ	SRC MHZ	PCI MHZ
0	0	1	133	100	33.3
0	1	1	166	100	33.3

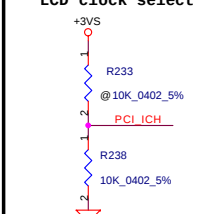
Table : ICS954306

FSB Frequency Selet:

CPU Driven *(Default)	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
	No Stuff	CLK_Rd	CLK_Re	CLK_Rf
533MHz	Stuff	CLK_Rd	CLK_Re	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
667MHz	Stuff	CLK_Rd	CLK_Rf	
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc

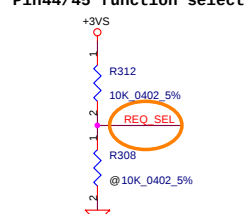


LCD clock select

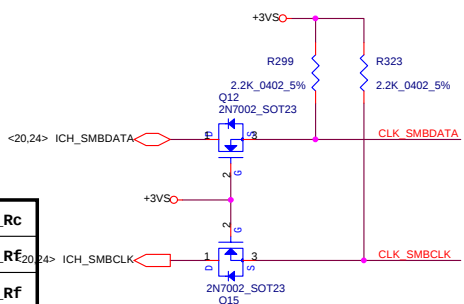


High: Pin18/19 = 100MHz
*Low: Pin18/19 = 96MHz

Pin44/45 function select



High: Pin44/45 = CLKREQ
*Low: Pin44/45 = CPUCLK2_ITP



<6/12> Remove CLK_48M_CB

<20> CLK_48M_ICH

<20> CLK_14M_ICH

<18> CLK_PCI_ICH

<2> CLK_PCI_LAN

<6/3> PCI CLK LAN selection (33MHz)

<31> CLK_PCI_EC

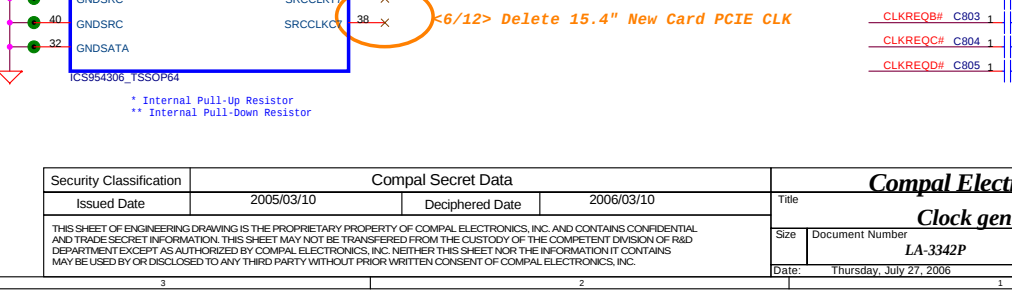
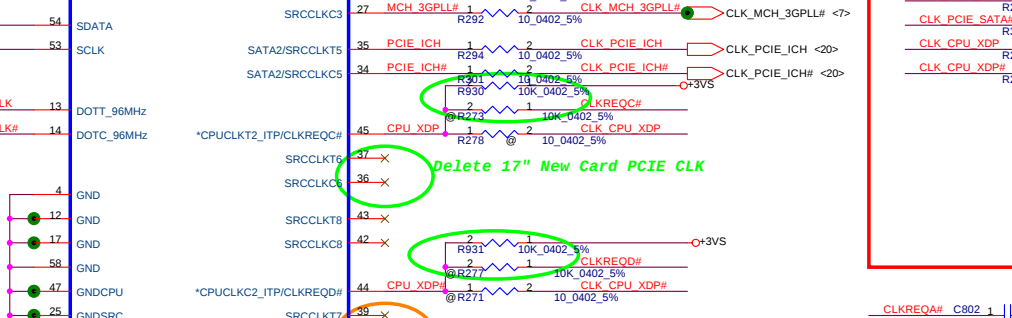
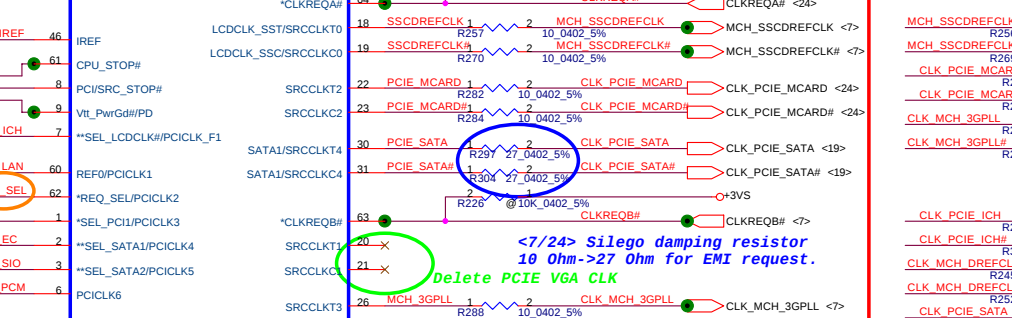
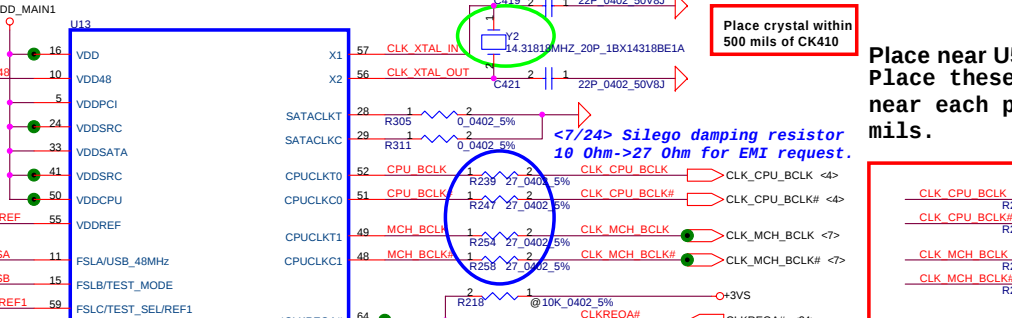
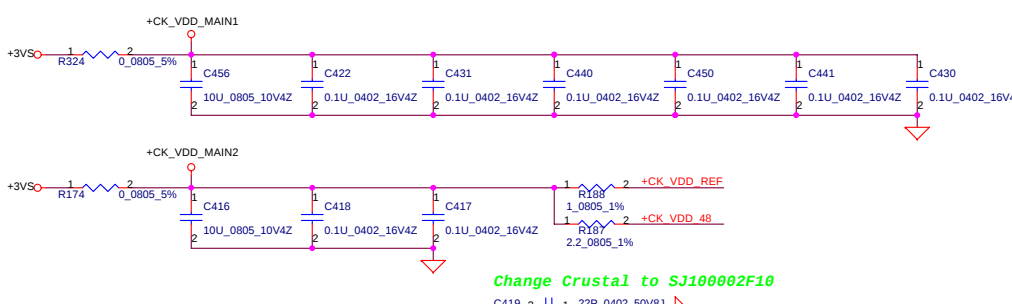
<29> CLK_PCI_SIO

<13,14> CLK_SMBDATA

<13,14> CLK_SMBCLK

<7> CLK_MCH_DREFCLK

<7> CLK_MCH_DREFCLK#



Change Crustal to SJ100002F10

Place crystal within 500 mils of CK410

<7/24> Silego damping resistor 10 Ohm->27 Ohm for EMI request.

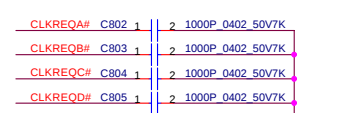
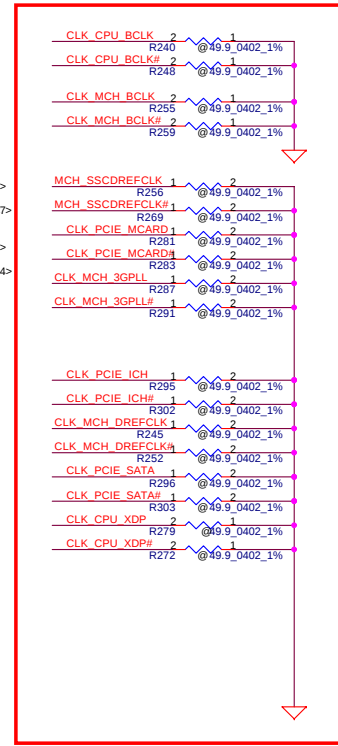
<7/24> Silego damping resistor 10 Ohm->27 Ohm for EMI request.

Delete PCIE VGA CLK

Delete 17" New Card PCIE CLK

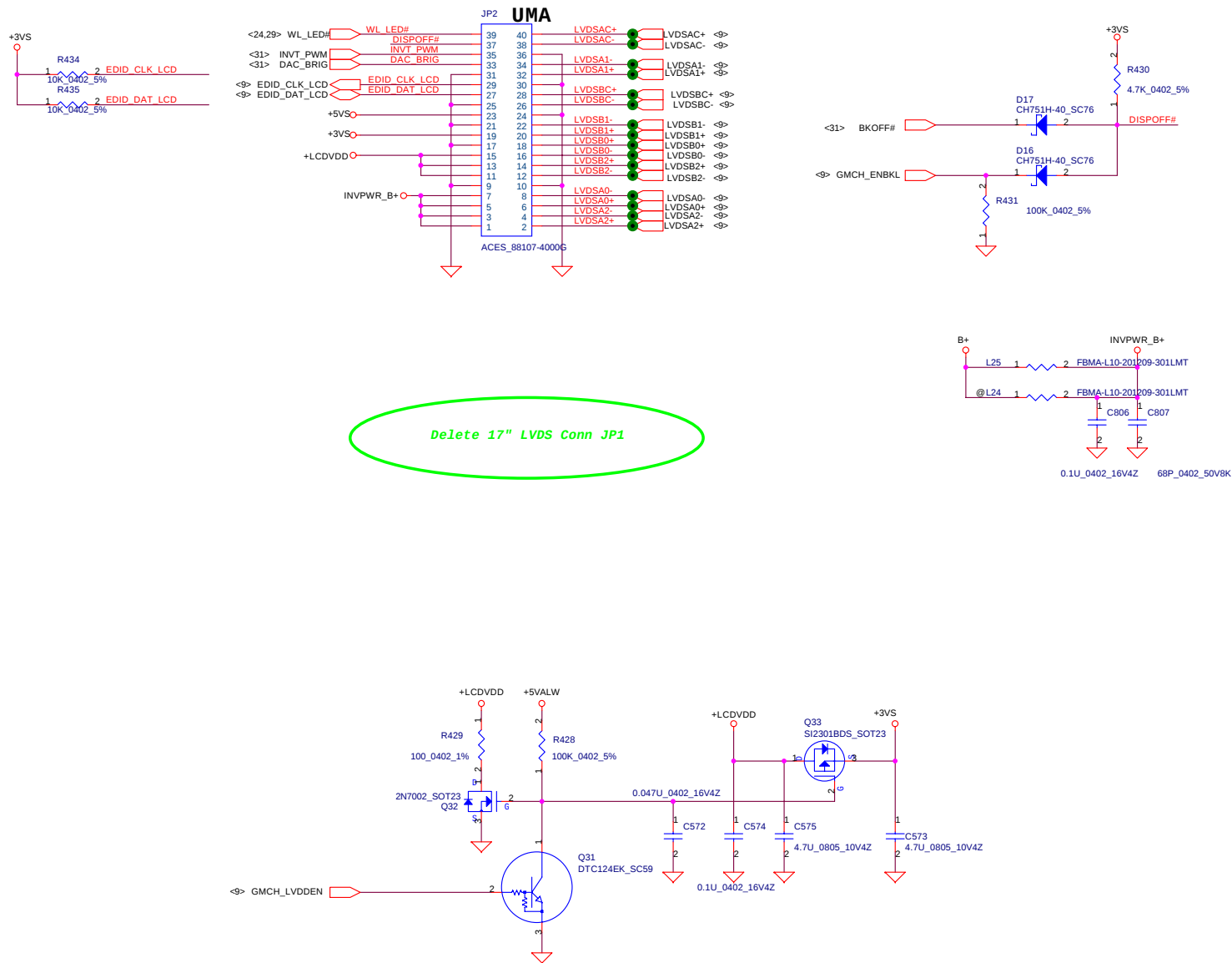
<6/12> Delete 15.4" New Card PCIE CLK

Place near U54
Place these components near each pin within 40 mils.

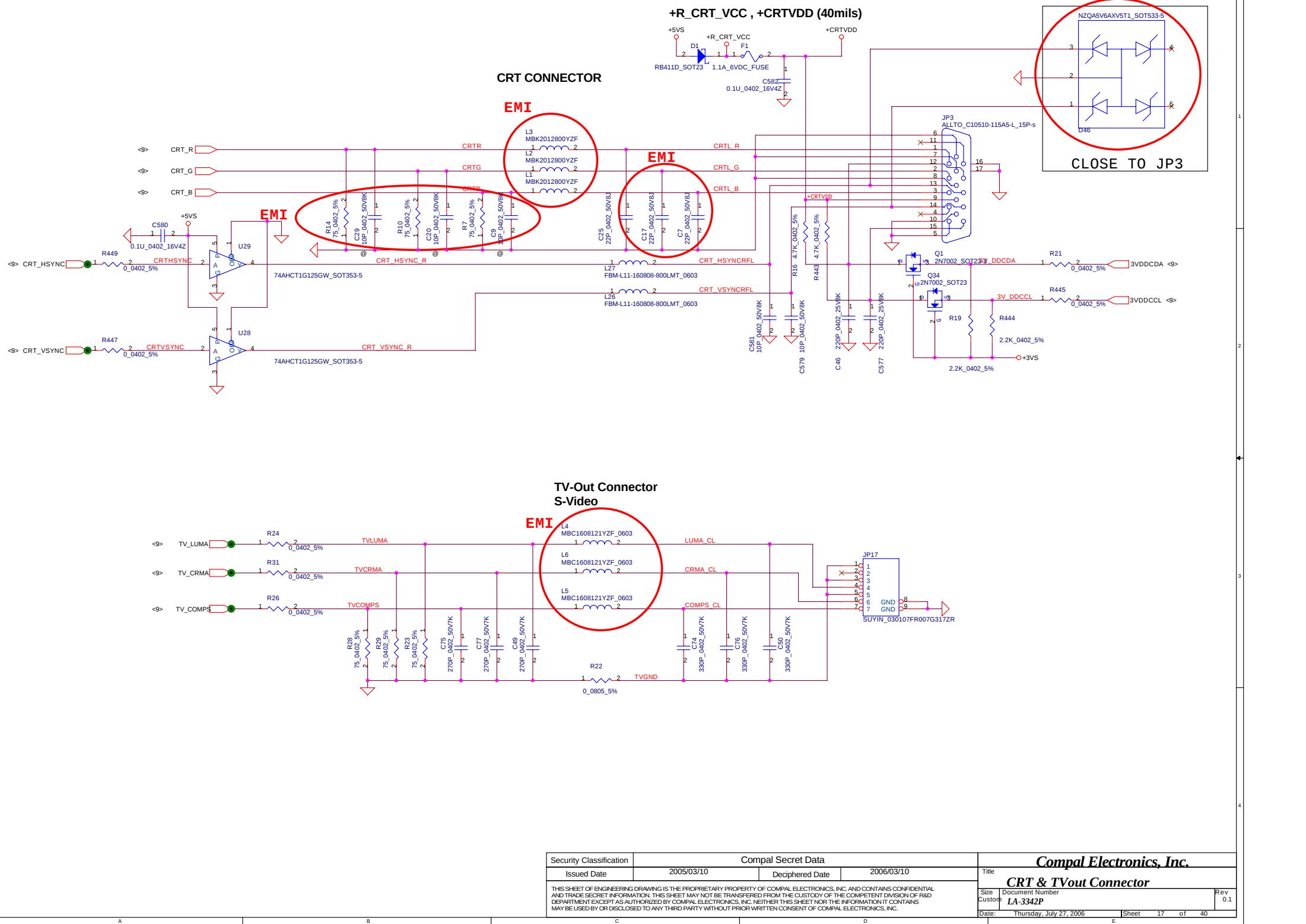


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					Size	Document Number	Rev
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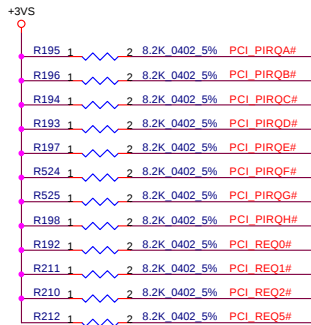
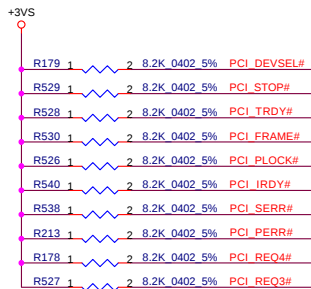
LCD Panel & inverter Connector



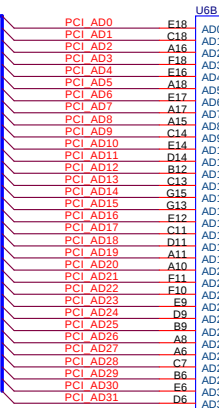
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				Custom	LA-3342P
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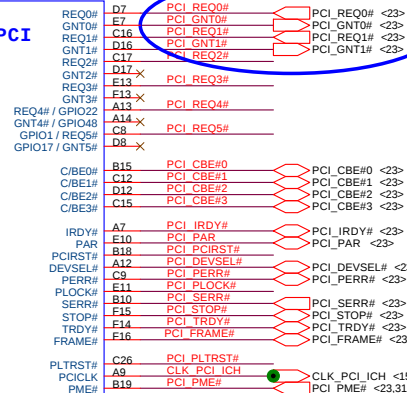
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Issued Date		Deciphered Date		2006/03/10	
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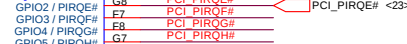
<23> PCI_AD[0..31]



PCI



Interrupt I/F

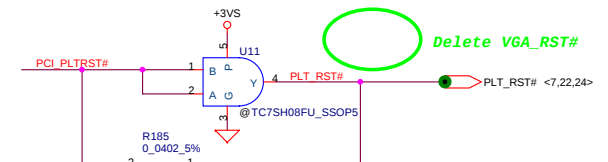
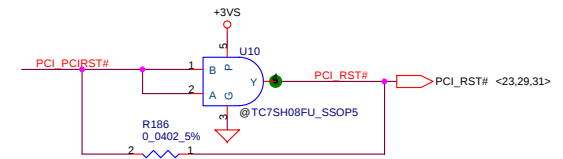


MISC



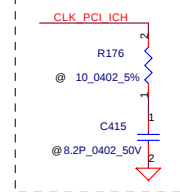
ICH7_BGA652-D

<7/20>Add option resistor for poor LAN performance.



Delete VGA_RST#

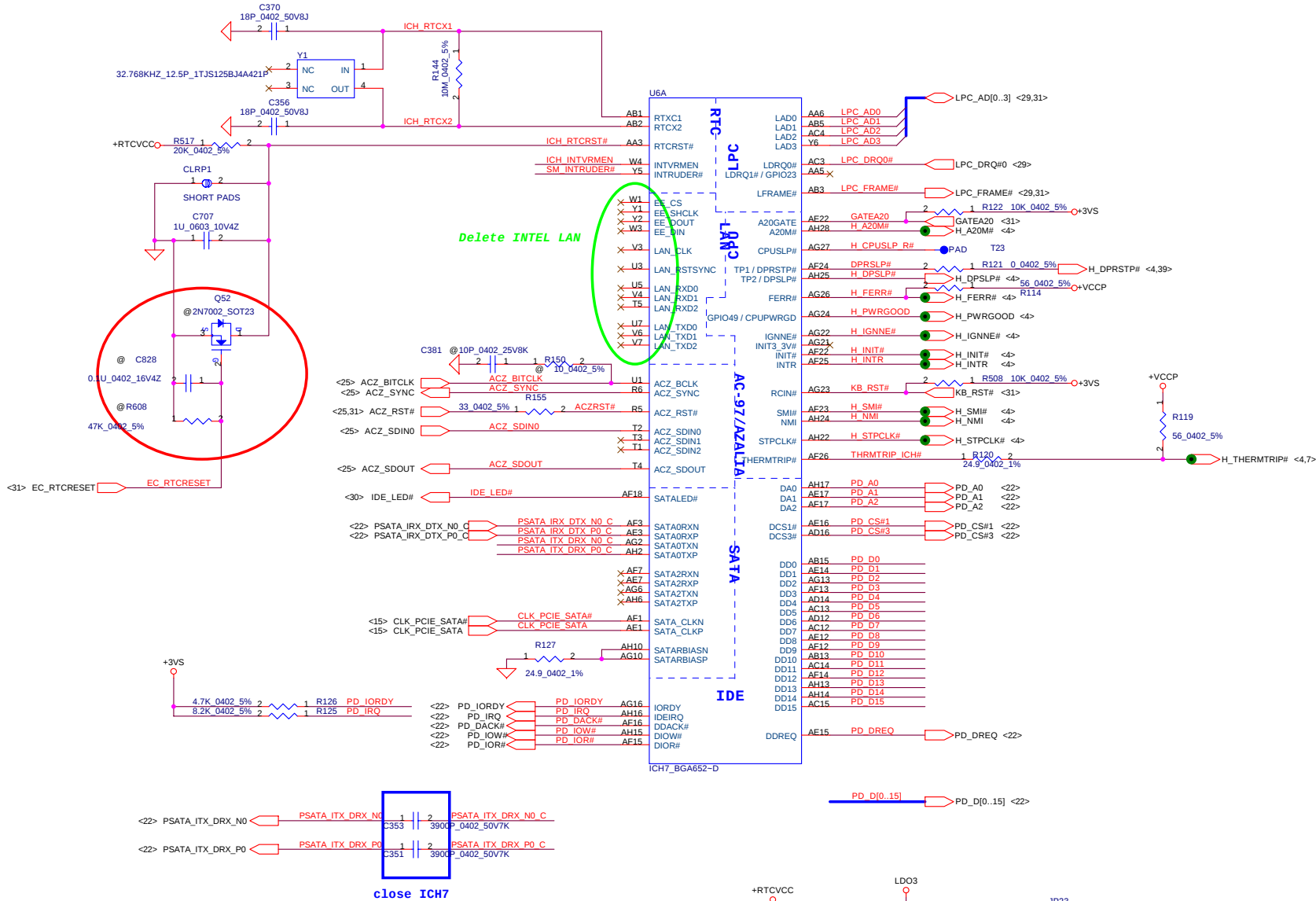
Place closely pin A9

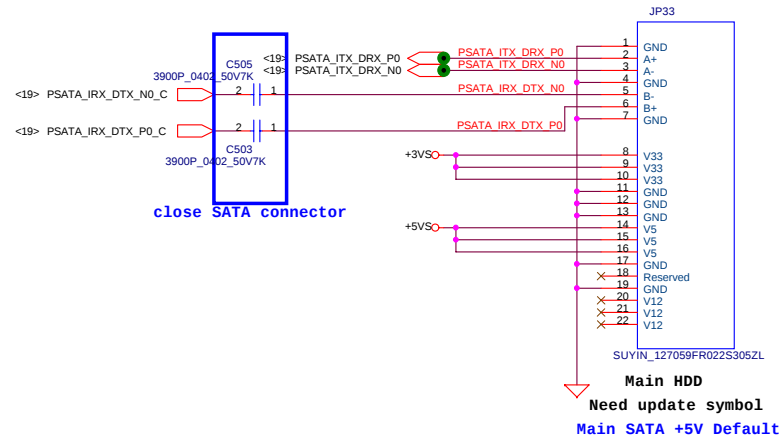
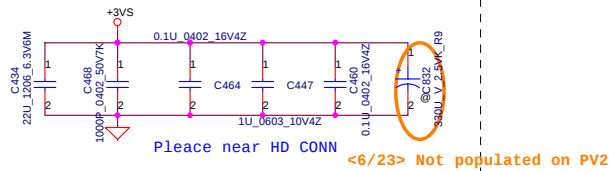
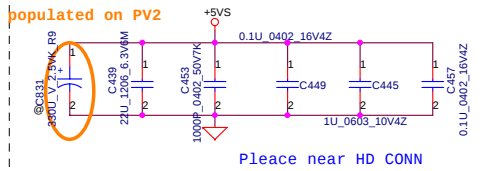


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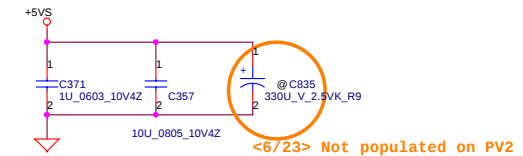
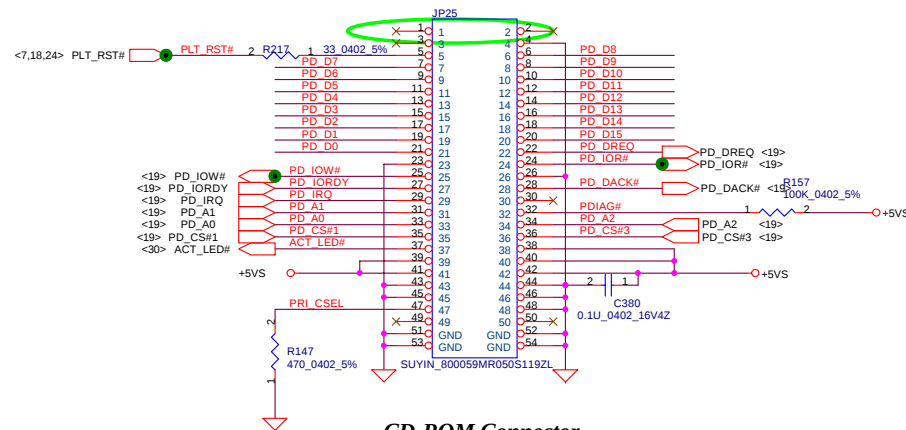
ICH7-M(1/4)

Rev 0.1

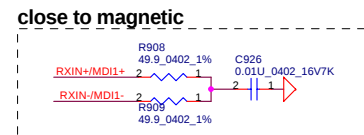
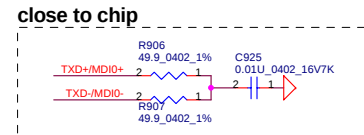
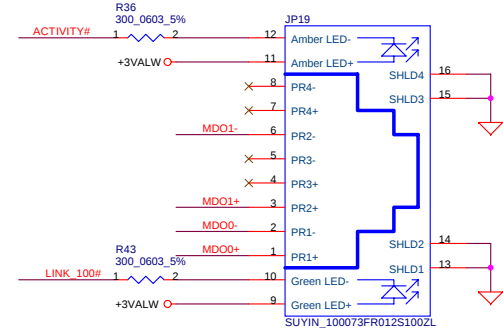
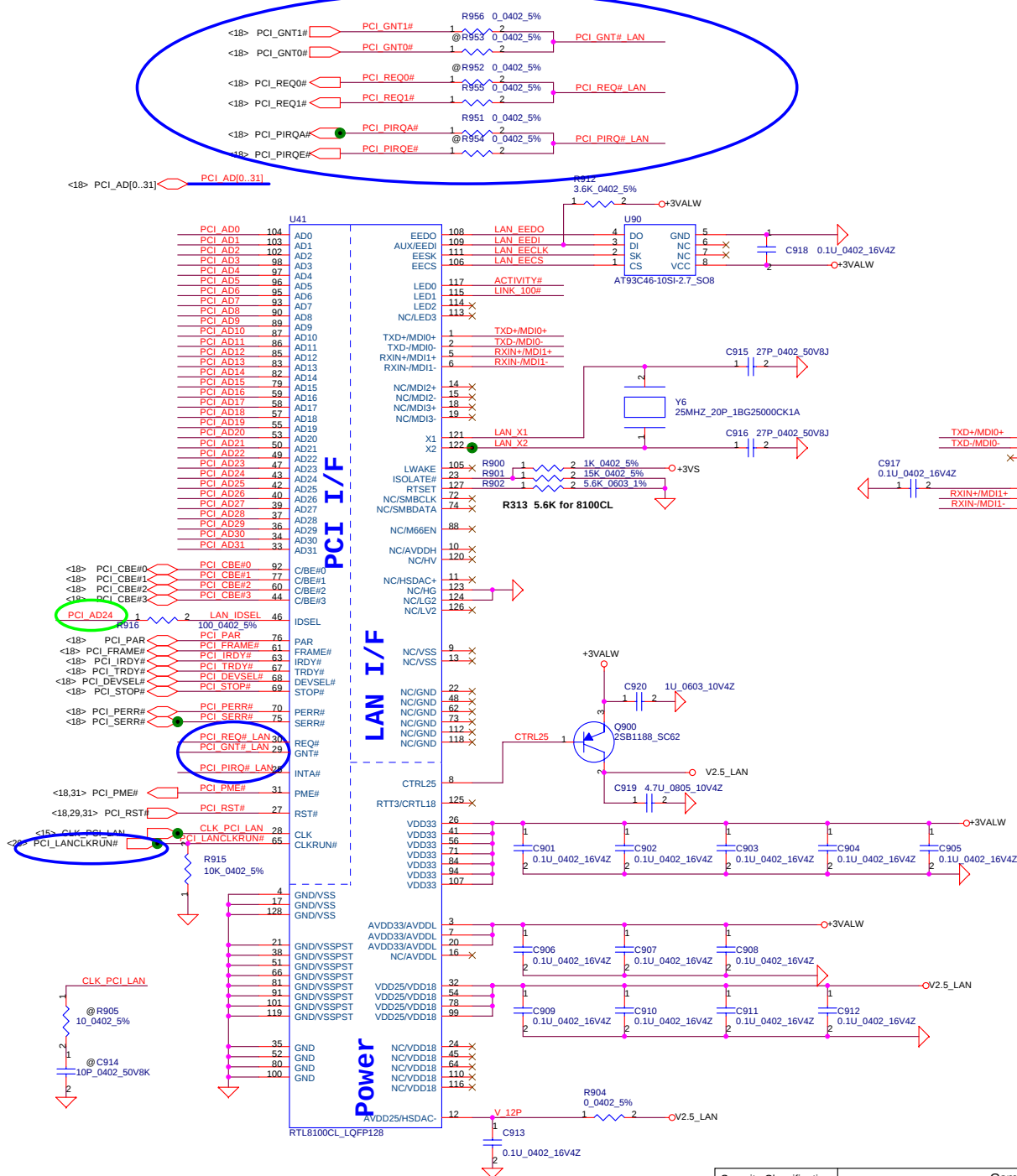




Delete CD traces (JP25 pin1,2 and3)

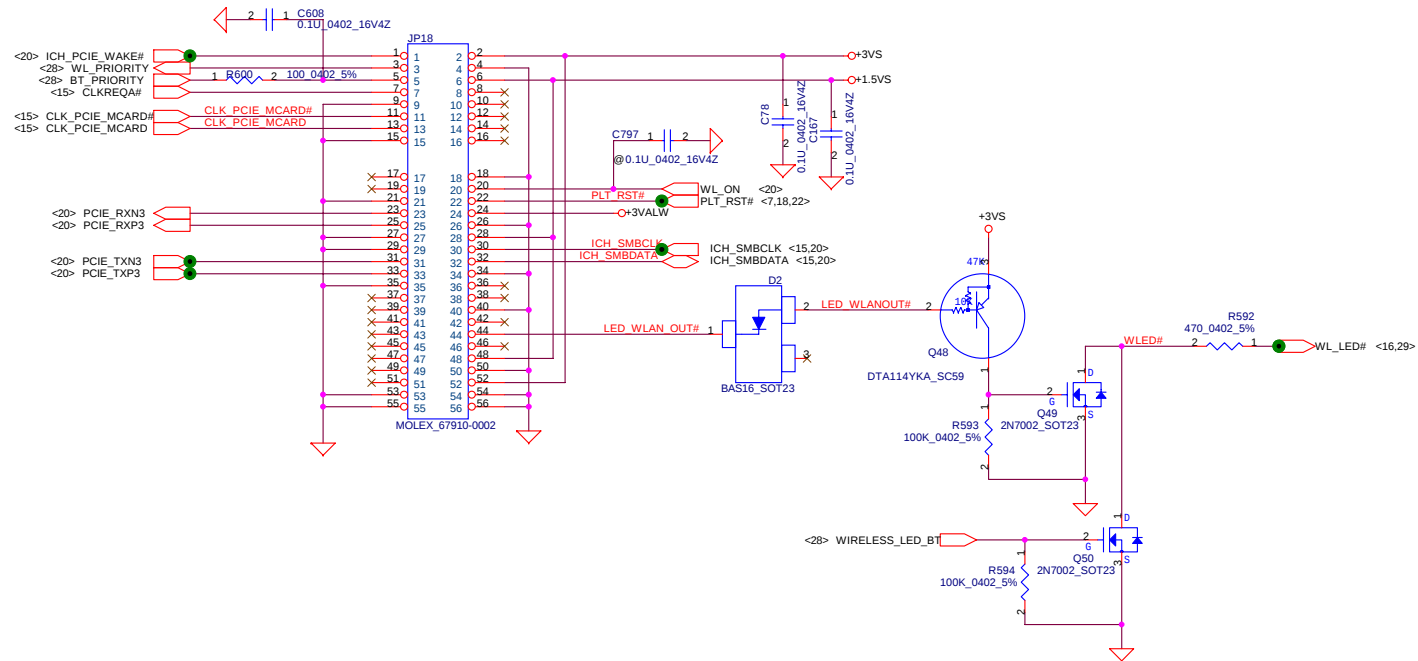


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Mini-Express Card(Slot 1-WLAN)



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<6/12> Remove PCM_SPK

For Layout:

Place decoupling caps near the power pins of SmartAMC device.

Delete CD traces

<6/12> Remove Docking line out

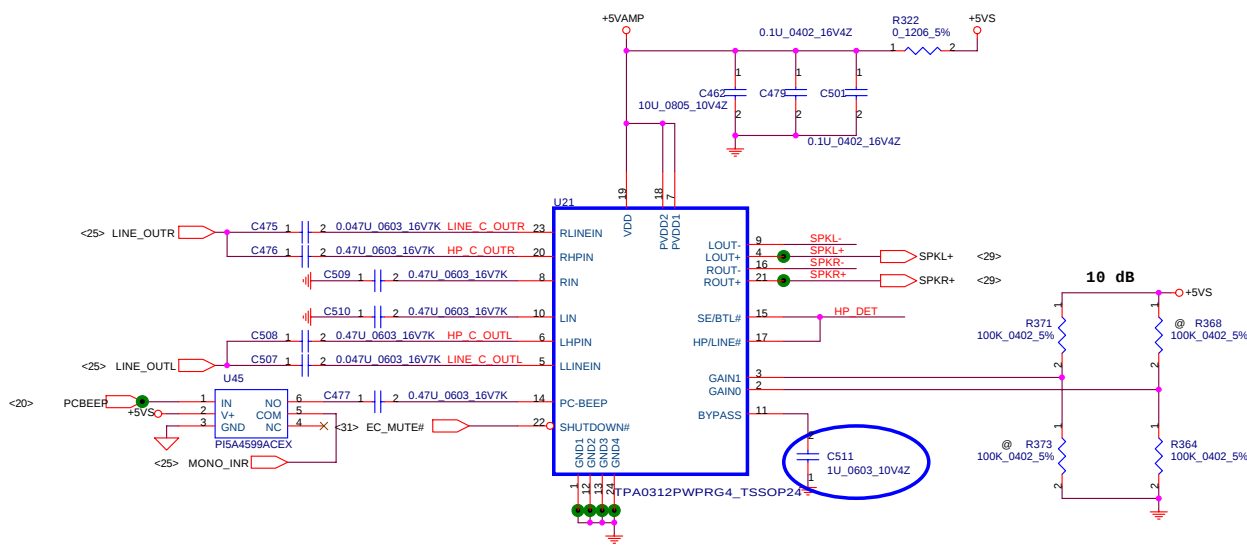
<6/12> Remove Docking MIC

<6/12> Remove JACK_DET from Docking

HP_DET#	JACK_DET#	PORT-A	PORT-B	EQ
0	0	ON	OFF	Disable
0	NC	ON	OFF	Disable
NC	0	OFF	ON	Disable
NC	NC	ON	OFF	Enable

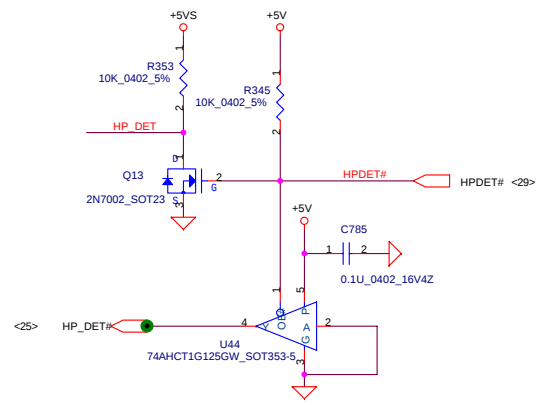
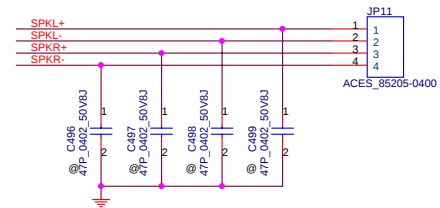
MIC_DET	PORT-C	PORT-F
0	ON	OFF
NC	OFF	ON

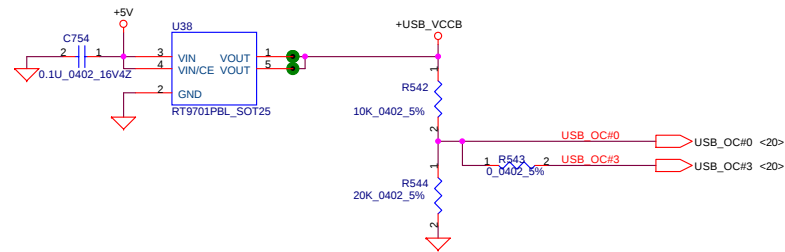
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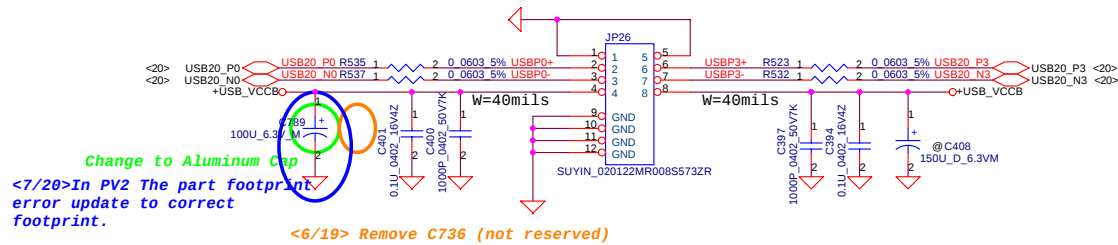
HEADPHONE OUT/LINE OUT

Gain Settings			
GAIN0	GAIN1	SE/BTL#	Av(inv)
0	0	0	6 dB
0	1	0	* 10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB



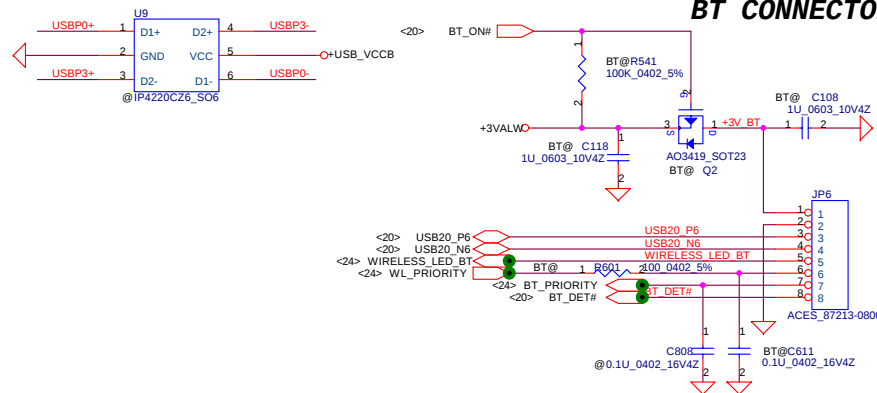


USB CONNECTOR (Left side)



BT CONNECTOR

Reserve Bluetooth

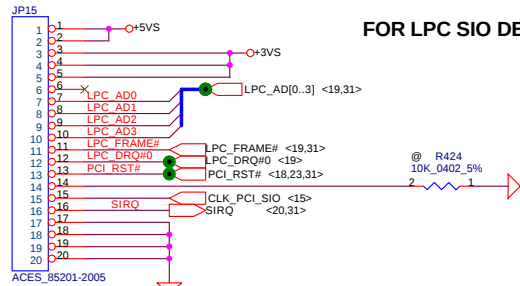


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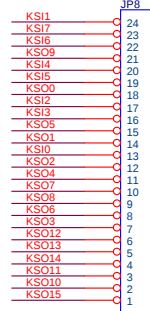
KSI[0..7] <31>
KSO[0..16] <31>

<31> KSO_D_17 <KSO_D_17>

FOR LPC SIO DEBUG PORT

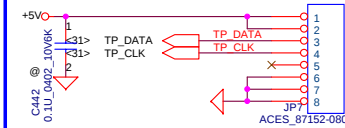


15.4 (TYPE "C" KB)

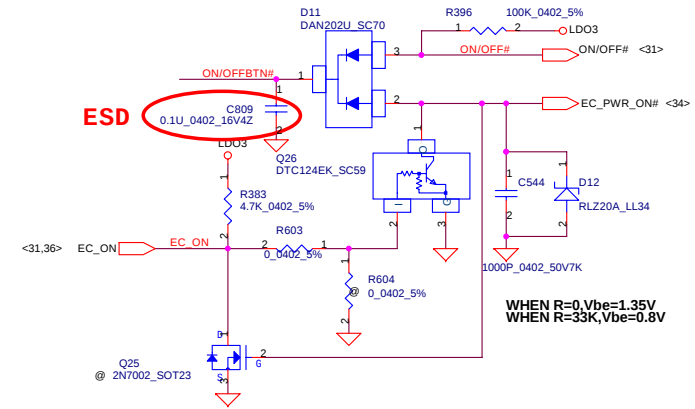


ACES_85201-2405

TP to MB CONN(15.4)

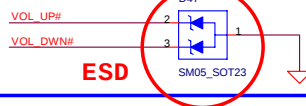
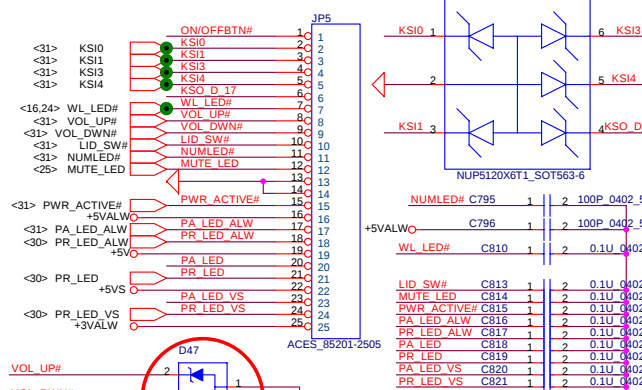


Power BTN

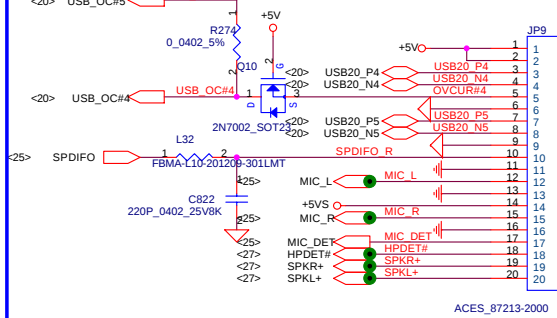


<6/21> Remove CIR

Switch board conn



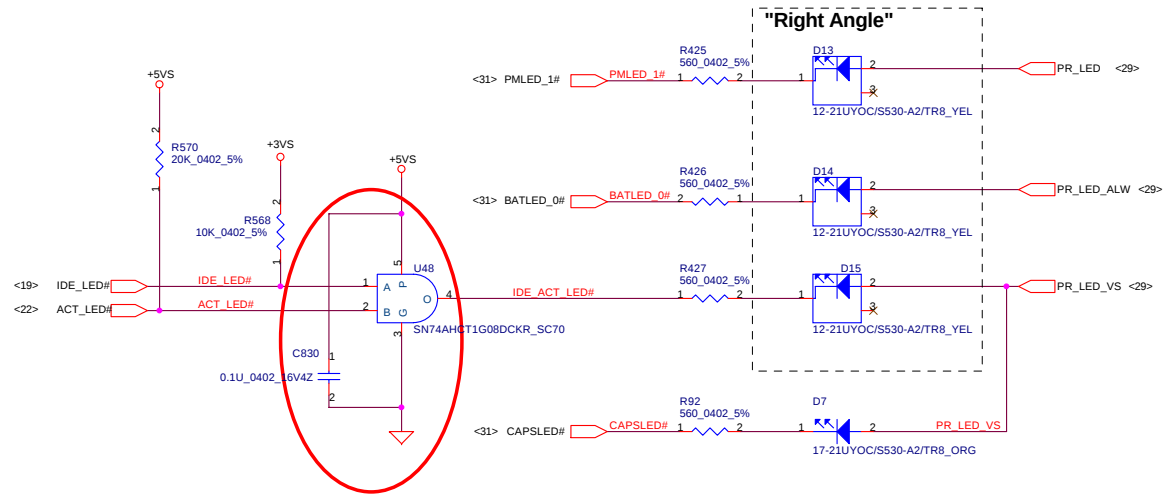
Audio board conn



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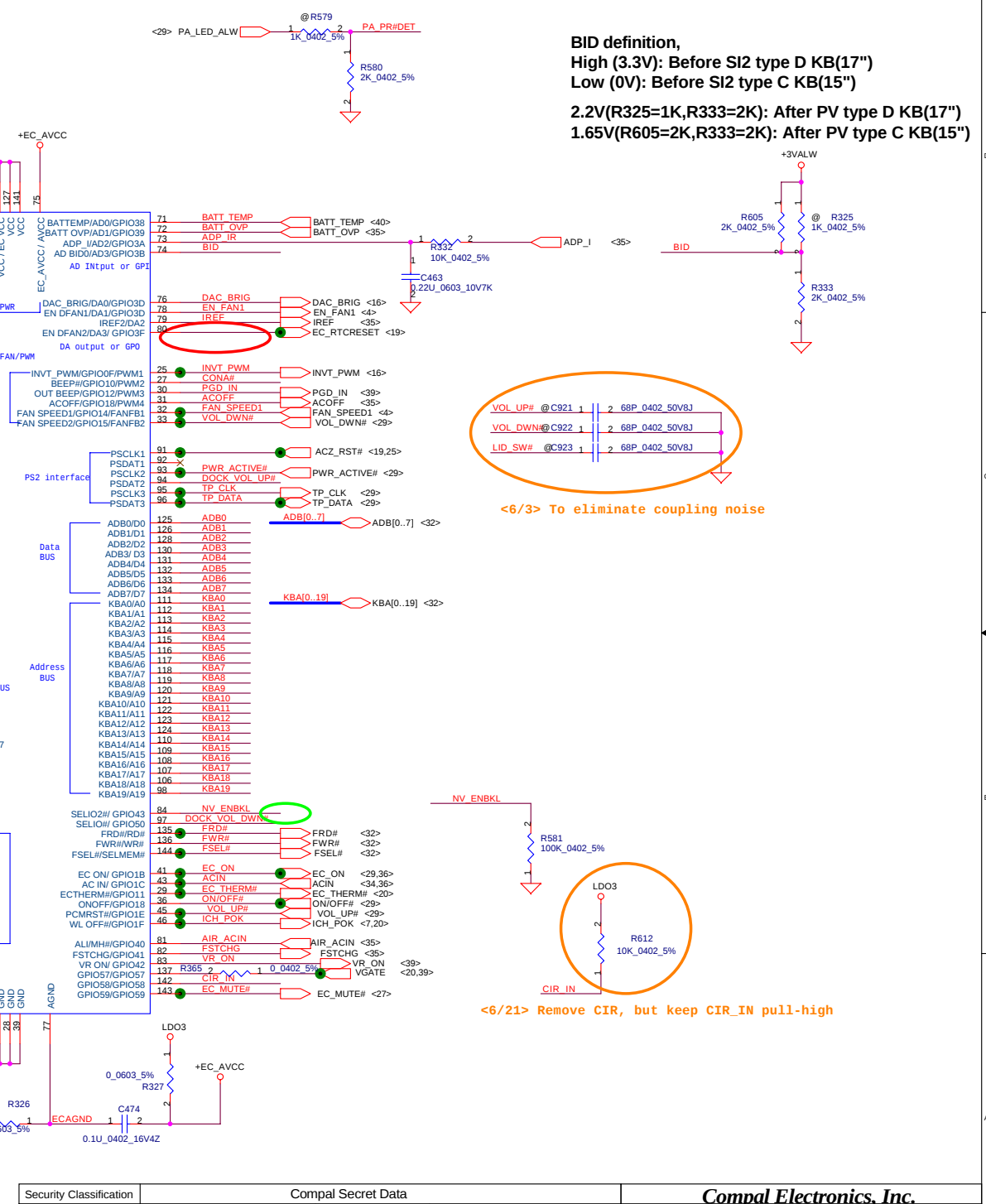
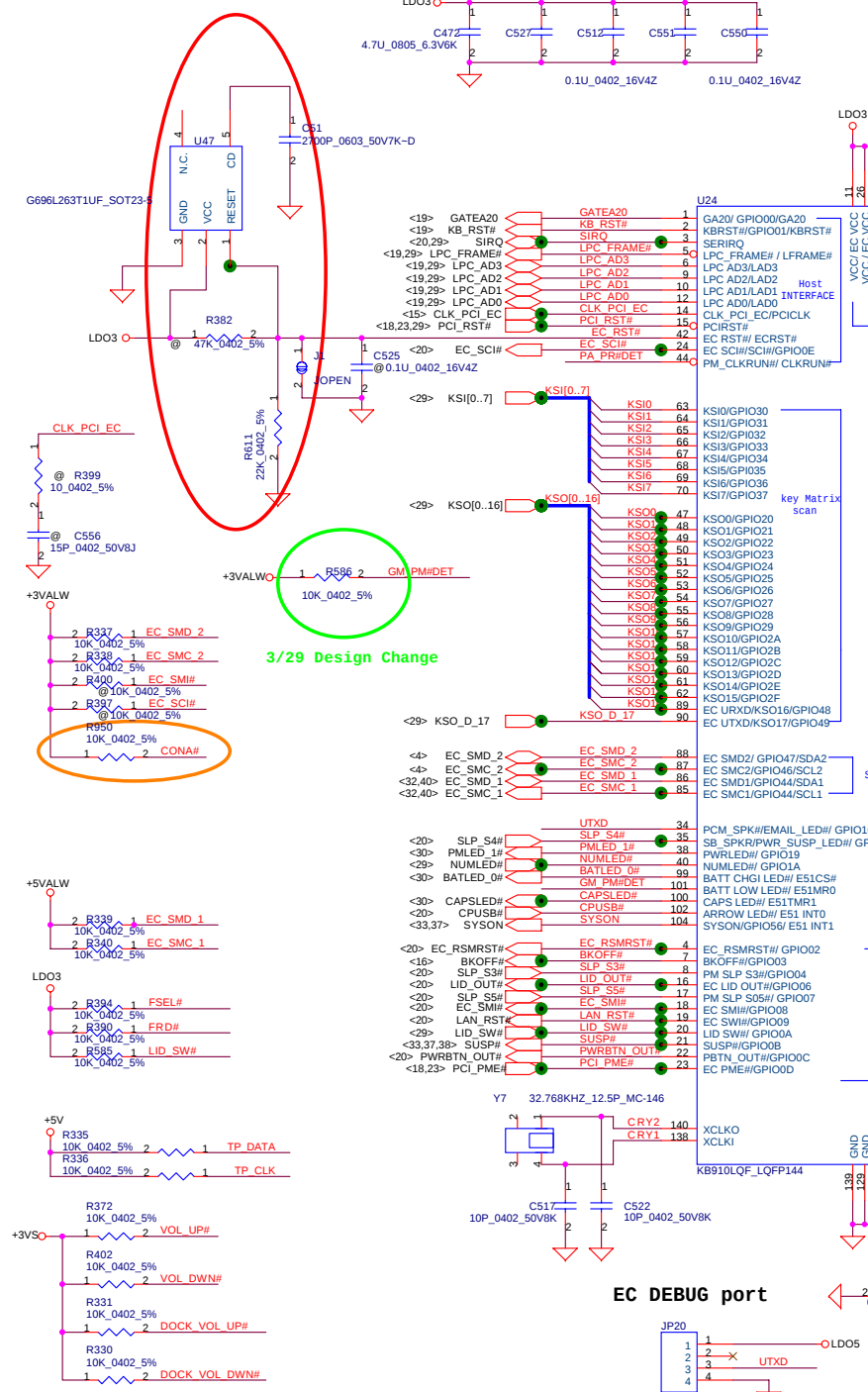
For PR

FOR POWER BUTTON BACKLIGHT SYSTEM POWER



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Cd(uF)=T(ms) / 1685
Cd=2700PF -----> T=3.6ms

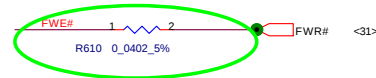
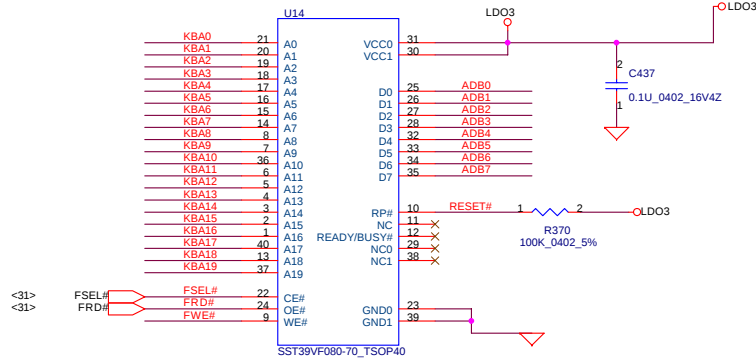
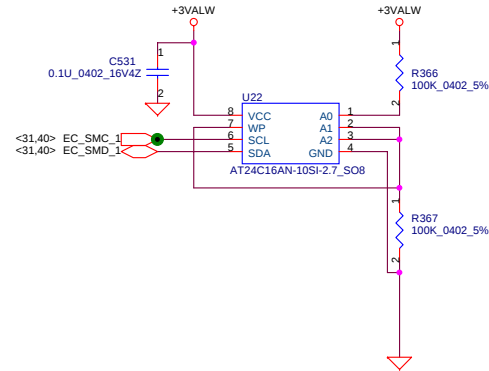
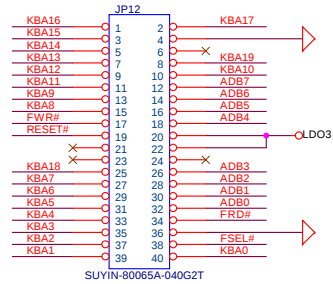


BID definition,
High (3.3V): Before SI2 type D KB(17")
Low (0V): Before SI2 type C KB(15")

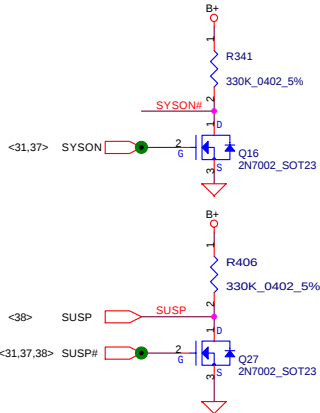
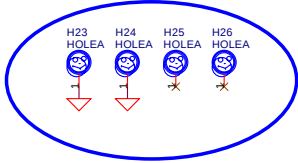
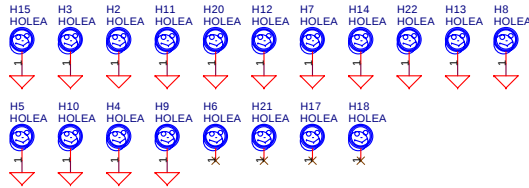
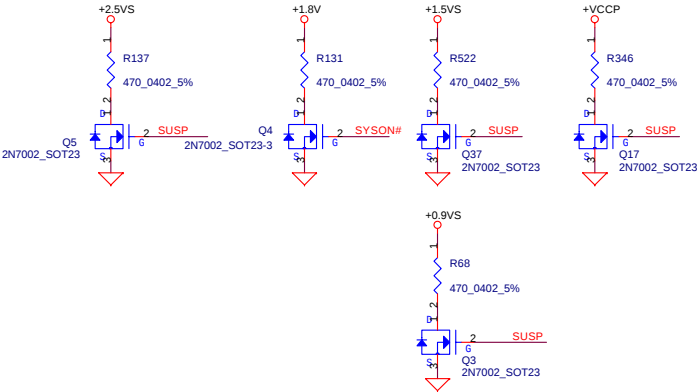
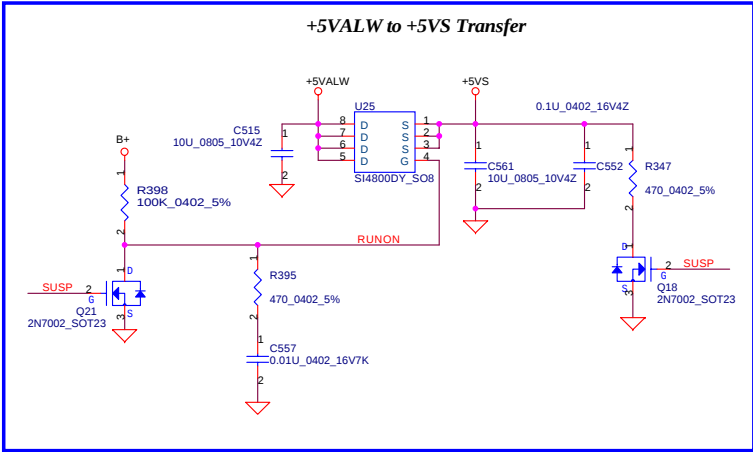
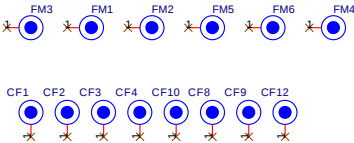
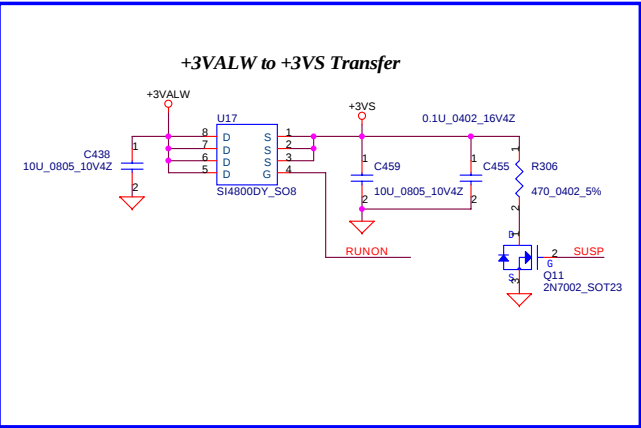
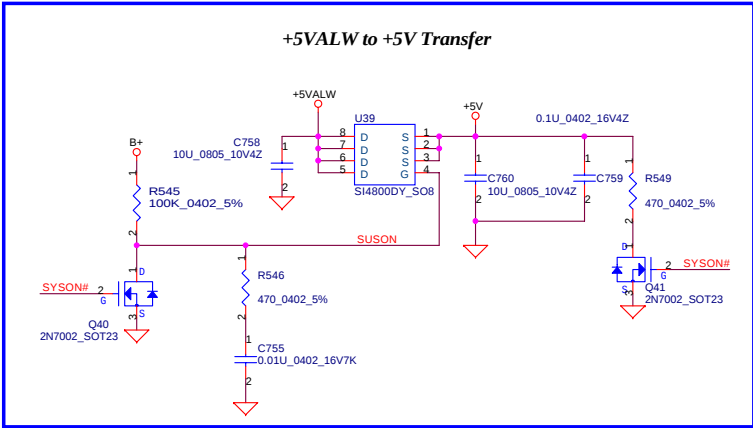
2.2V(R325=1K,R333=2K): After PV type D KB(17")
1.65V(R605=2K,R333=2K): After PV type C KB(15")

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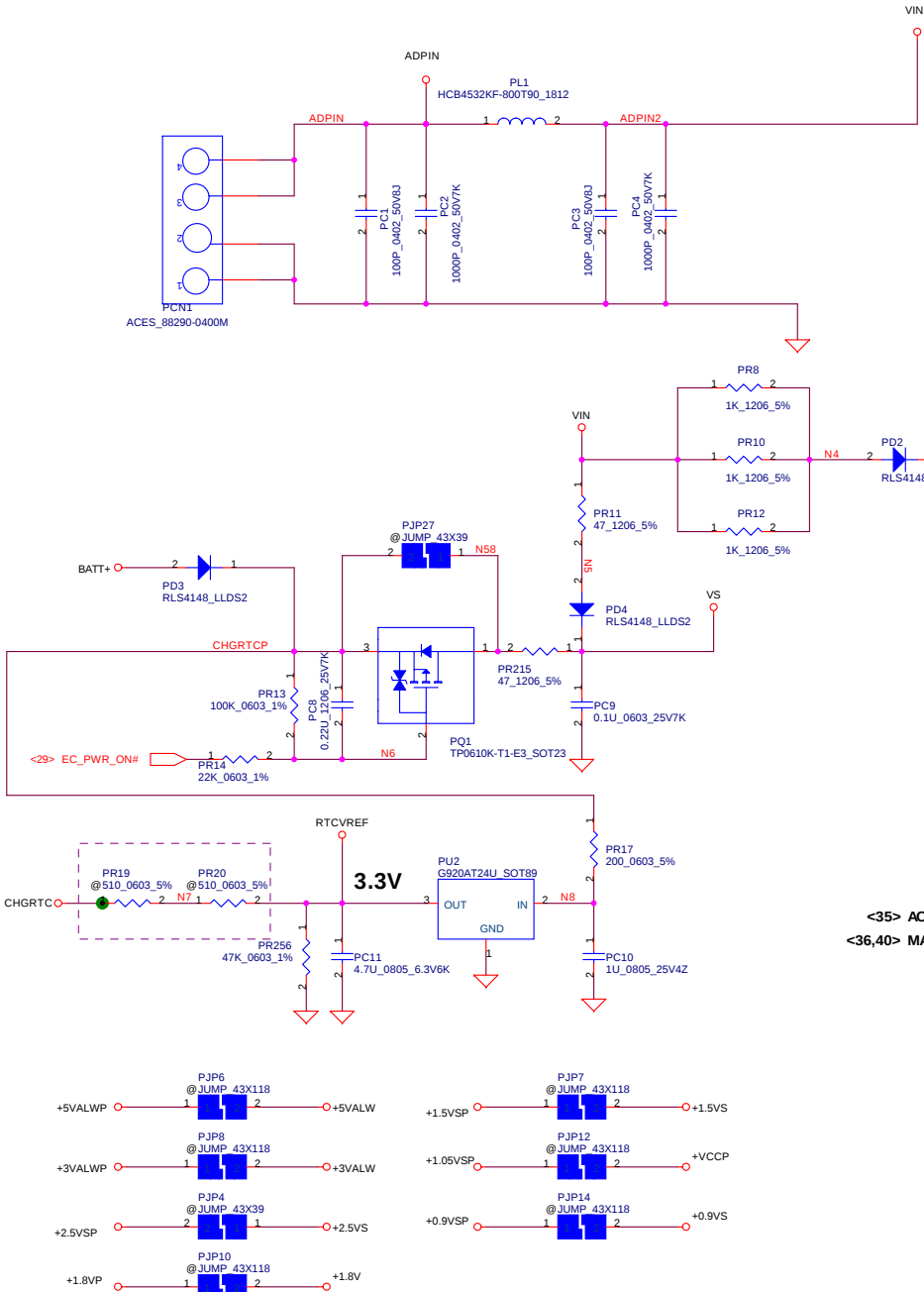
<31> ADB[0..7] ADB[0..7]
<31> KBA[0..19] KBA[0..19]



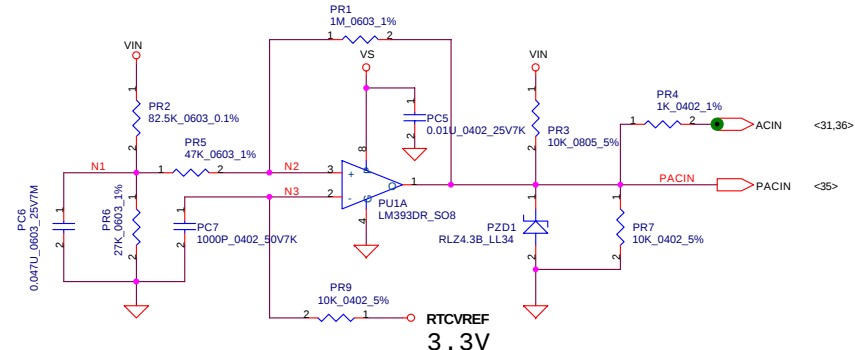
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				Date:	Thursday, July 27, 2006
				Sheet	33 of 40
				Rev	0.1

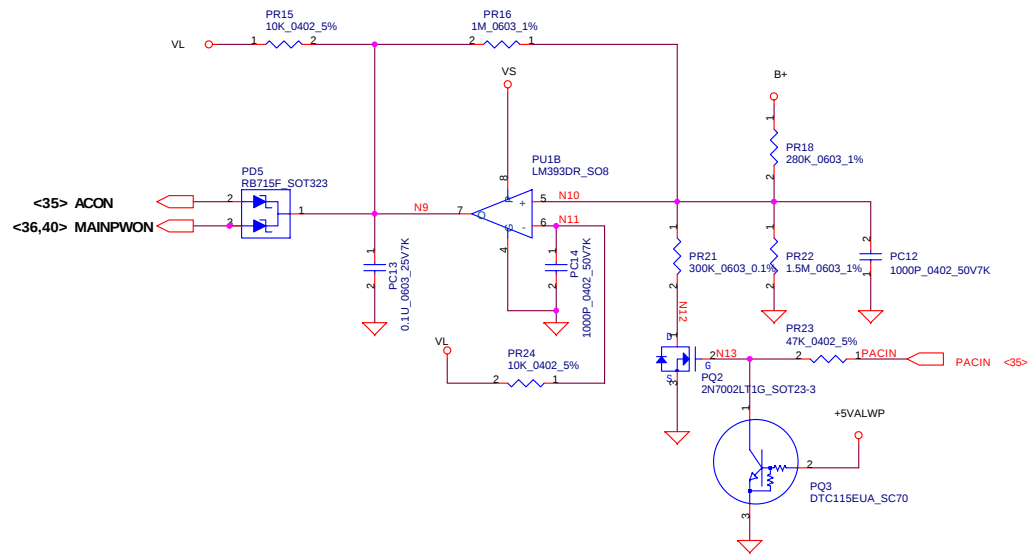


Vin Detector :			
14.698	14.285	13.879	
13.818	13.411	13.000	



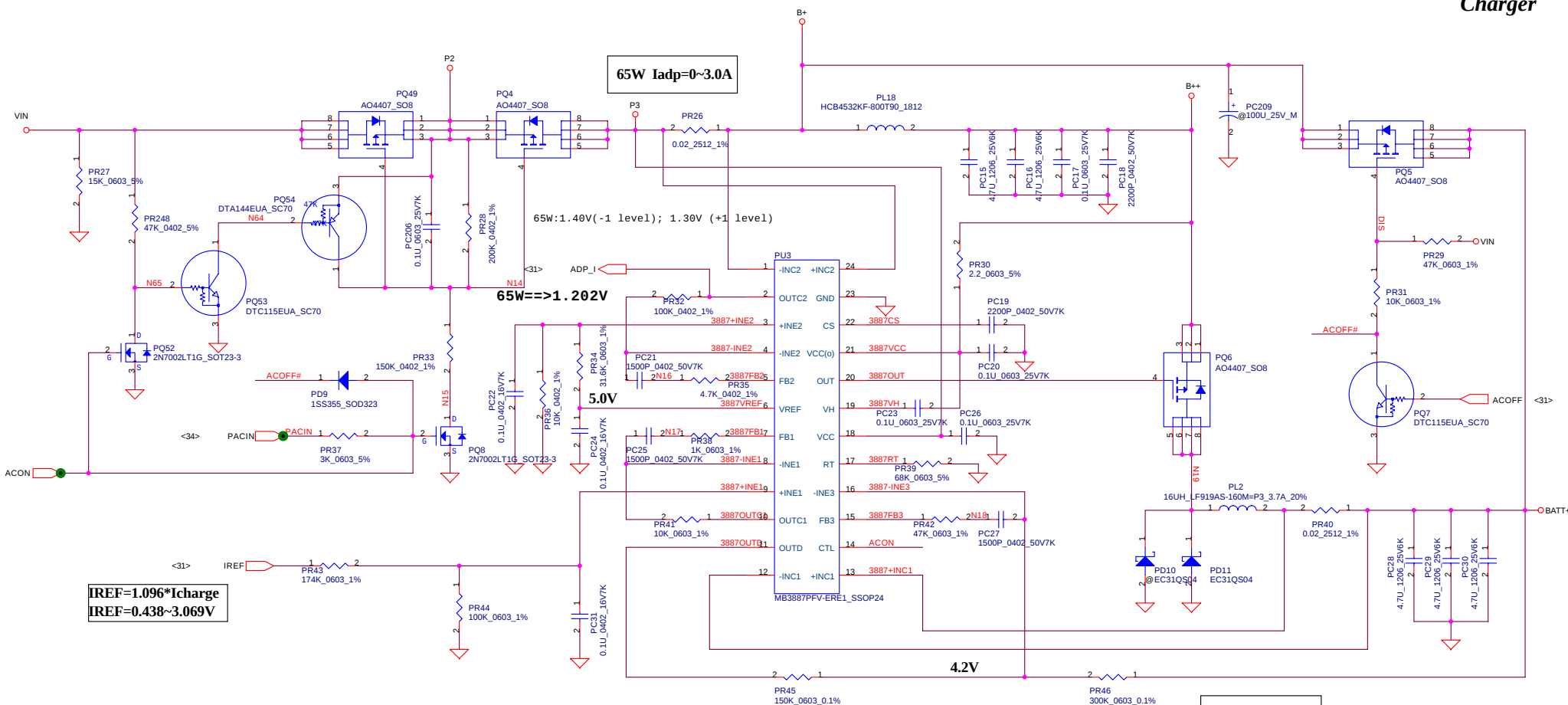
ACIN:			
Precharge detector			
12.384	12.000	11.624	
10.927	10.600	10.223	

BATT			
Precharge detector			
7.558	7.333	7.112	
6.108	5.933	5.704	

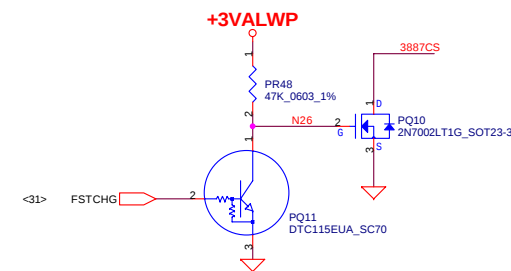
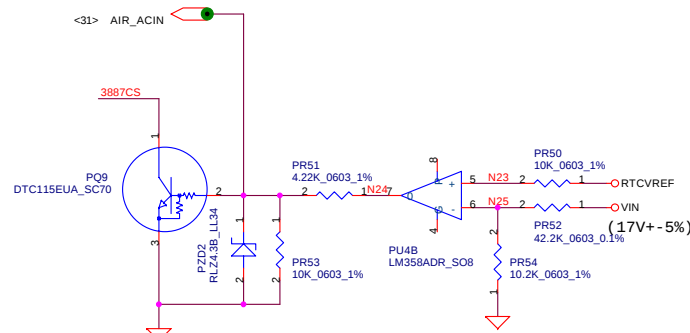
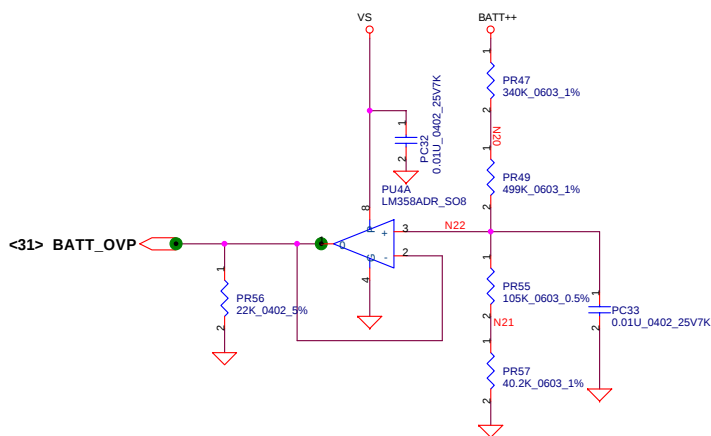


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				Size		Document Number	
				Customer		Rev	
						0.2	
				Date:		Thursday, July 27, 2006	

Charger

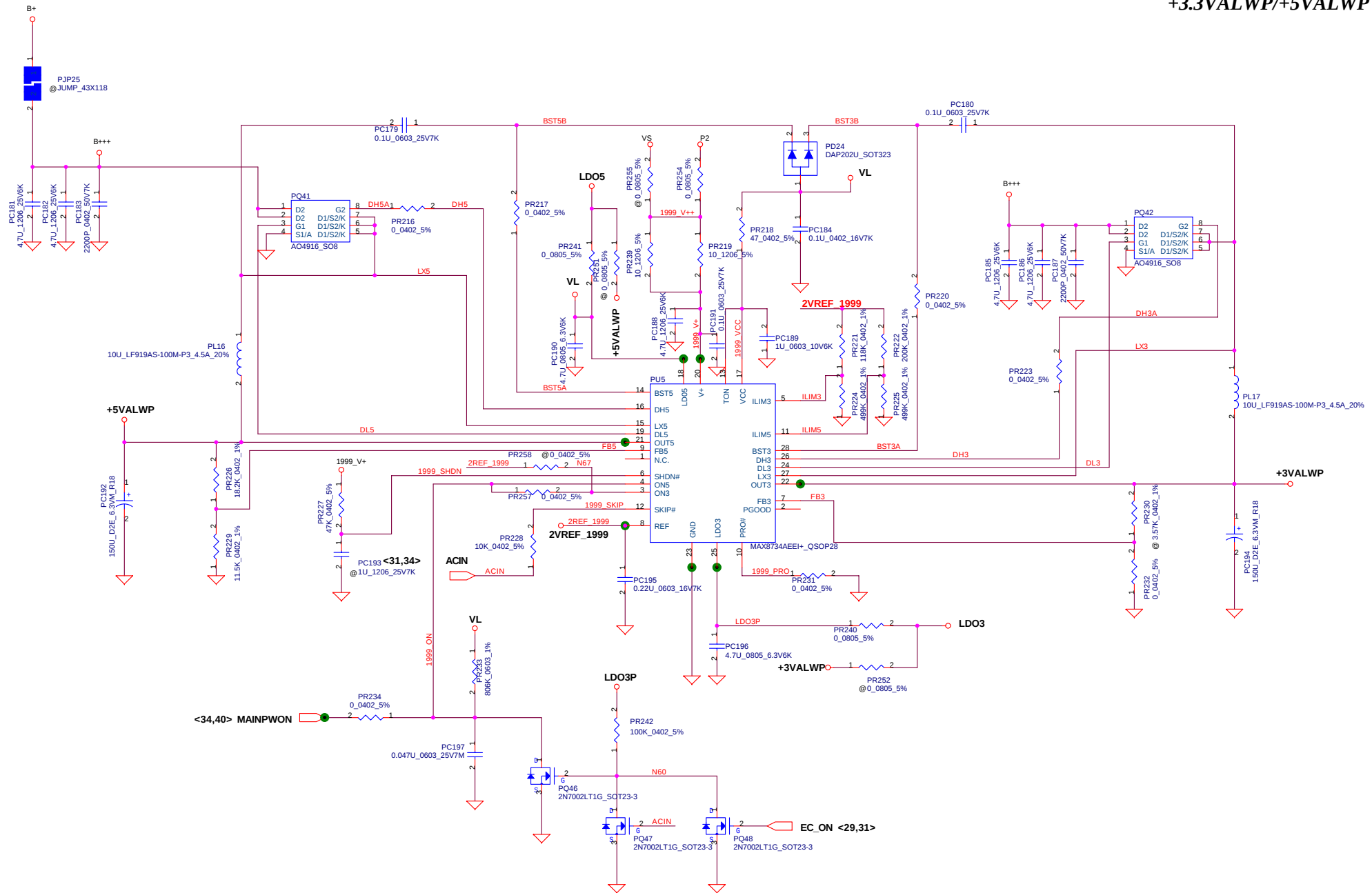


3S2P/3S4P : 13.5V--> BATT_OVP= 2.0V
(BAT_OVP=0.14753 *BATT+)



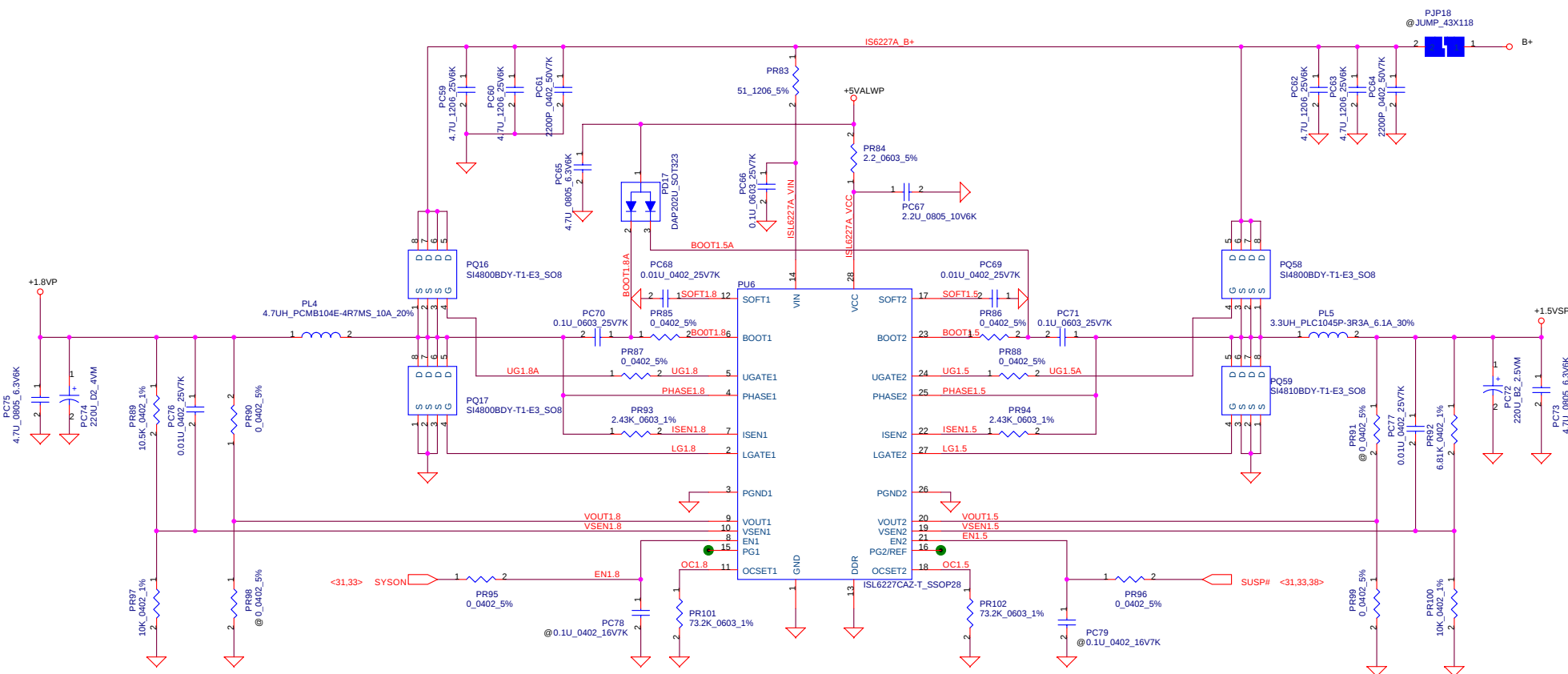
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+3.3VALWP/+5VALWP

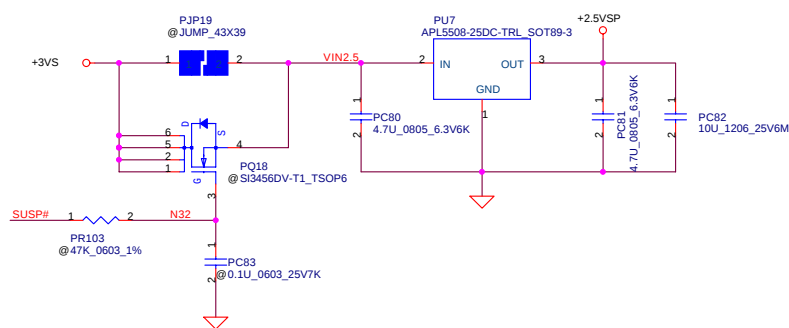


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				Date:	Thursday, July 27, 2006	Sheet 36 of 40

+2.5VSP/+1.8VP/+1.5VSP

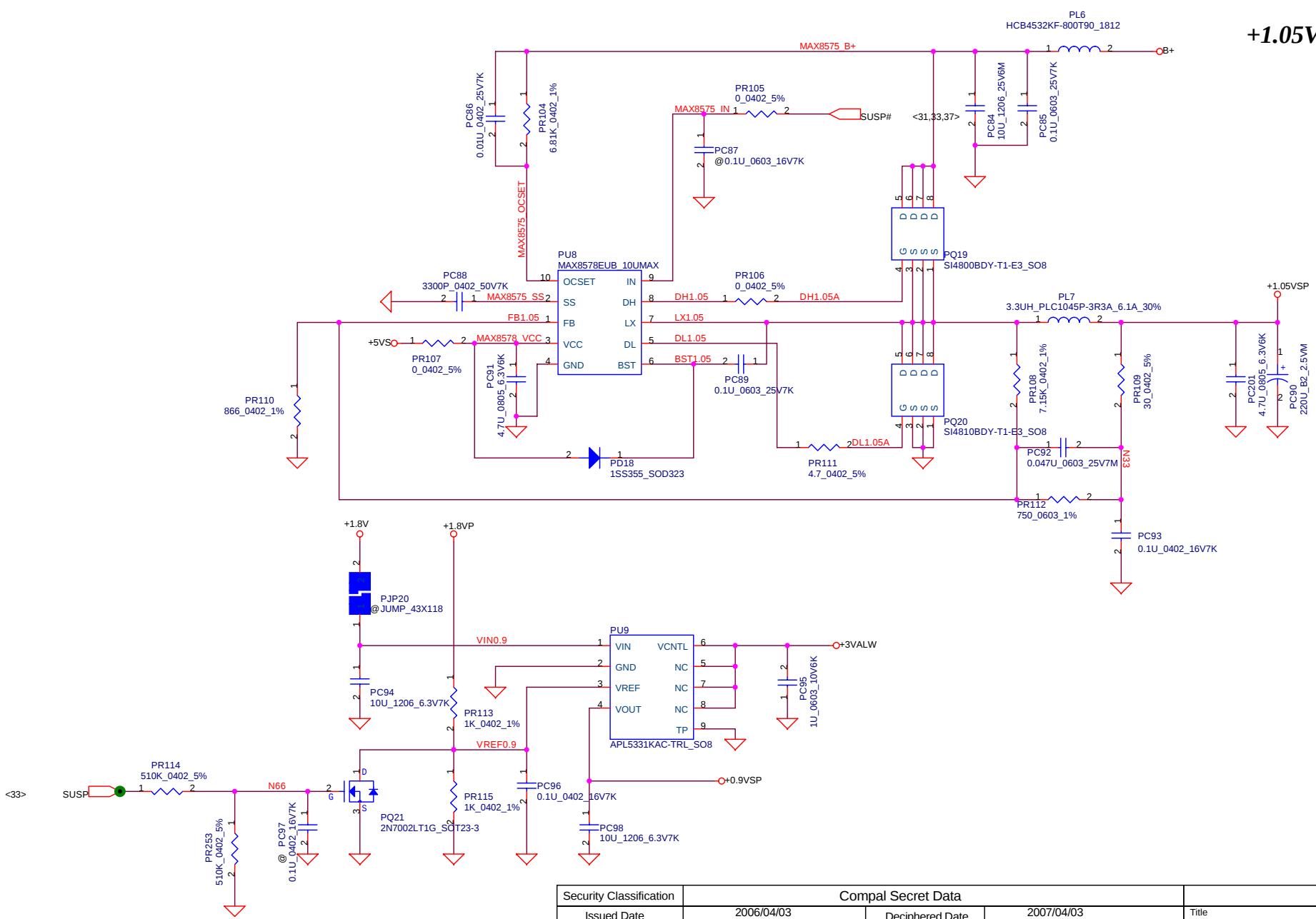


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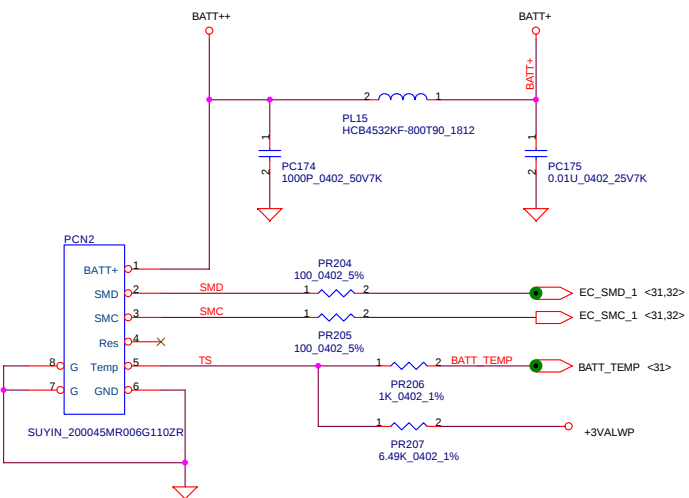


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				+2. 5VSP/+1. 8VP/+1. 5VSP	
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+1.05V_VCCPP/+0.9VSP

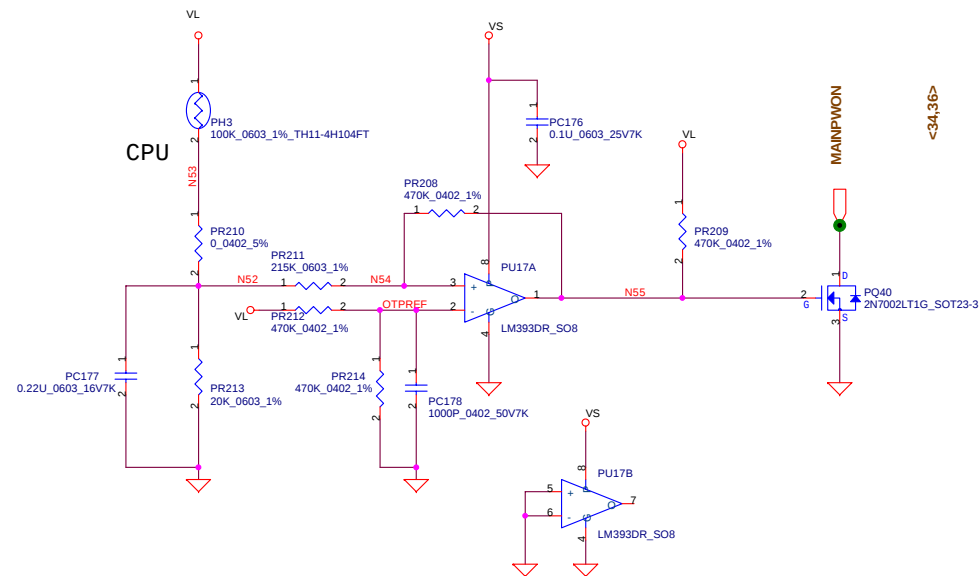


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PJPB1 battery connector
SMART
Battery:
1.BATT+
2.SMBD
3.SMBC
4.Res
5.Temp
6.GND

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C



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					Size	Document Number	Rev
					Custom	Information	
Date:		Thursday, July 27, 2006		Sheet	40 of 40		